426ball FBGA Specification

8Gb LPDDR3 (x32, 2-Channel)

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Document Title
FBGA
8Gb (x32, 2-Channel) LPDDR3

Revision History

Revision No.	History	Draft Date	Remark
0.1	- Initial Draft	Jun. 2014	Preliminary
0.2	- Changed Refresh command - Editorial Changes	Nov. 2014	Preliminary
0.3	- Updated IDD specification	Dec. 2014	Preliminary
1.0	Final Version - Updated IDD specification	Dec. 2014	

FEATURES

[FBGA]

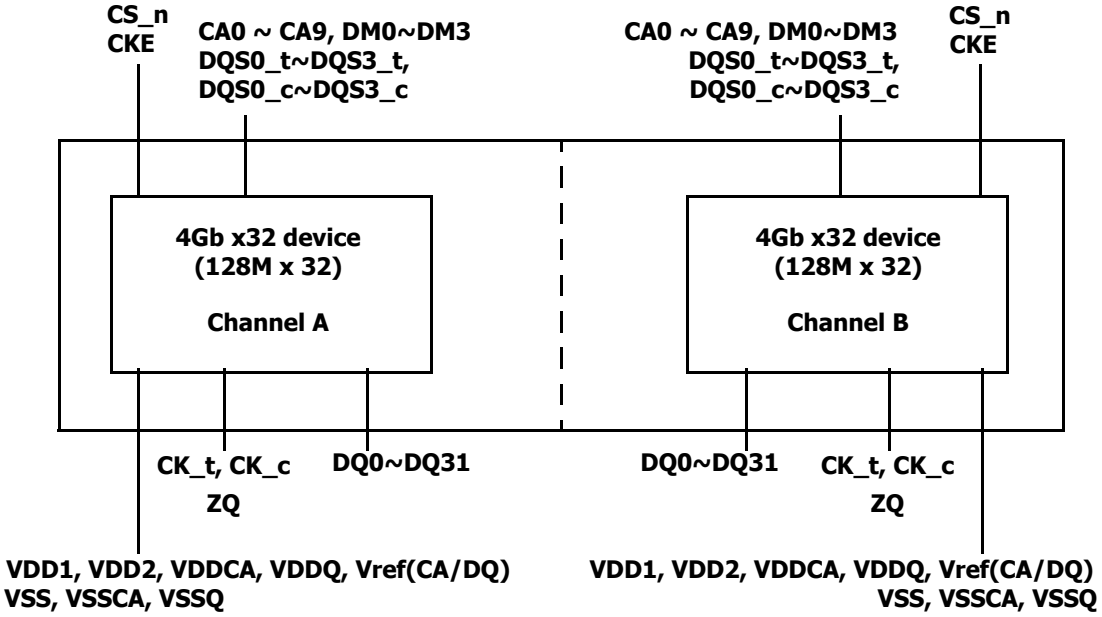
● Operation Temperature
- (-30)°C ~ 105°C

● Package
- 426-ball FBGA
- 13.5x14.5mm^2, 0.64t, 0.35mm pitch
- Lead & Halogen Free

[LPDDR3]

- VDD1 = 1.8V (1.7V to 1.95V)
- VDD2, VDDCA and VDDQ = 1.2V (1.14V to 1.30)
- HSUL_12 interface (High Speed Unterminated Logic 1.2V)
- Double data rate architecture for command, address and data Bus;
  - all control and address except CS_n, CKE latched at both rising and falling edge of the clock
  - CS_n, CKE latched at rising edge of the clock
  - two data accesses per clock cycle
- Differential clock inputs (CK_t, CK_c)
- Bi-directional differential data strobe (DQS_t, DQS_c)
  - Source synchronous data transaction aligned to bi-directional differential data strobe (DQS_t, DQS_c)
  - Data outputs aligned to the edge of the data strobe (DQS_t, DQS_c) when READ operation
  - Data inputs aligned to the center of the data strobe (DQS_t, DQS_c) when WRITE operation
- DM masks write data at the both rising and falling edge of the data strobe
- Programmable RL (Read Latency) and WL (Write Latency)
- Programmable burst length: 8
- Auto refresh and self refresh supported
- All bank auto refresh and per bank auto refresh supported
- Auto TCSR (Temperature Compensated Self Refresh)
- PASR (Partial Array Self Refresh) by Bank Mask and Segment Mask
- DS (Drive Strength)
- DPD (Deep Power Down)
- ZQ (Calibration)

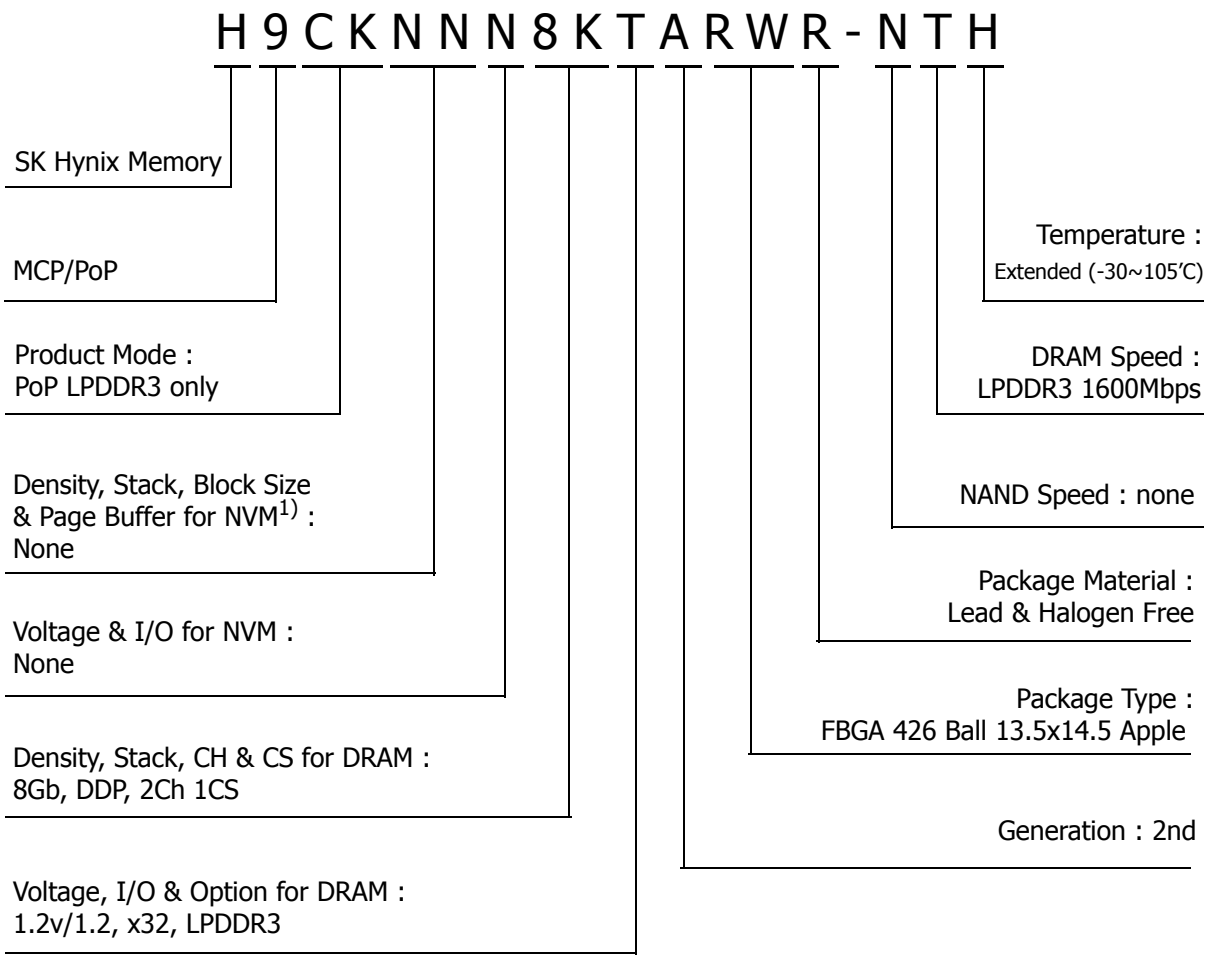
Functional Block Diagram



Note
1. Total current consumption is dependent to user operating conditions.

ORDERING INFORMATION

Part Number	Memory Combination	Operation Voltage	Density	Speed	Package
H9CKNNN8KTARWR-NTH	LPDDR3	1.8V/1.2/1.2/1.2	8Gb (x32, 2Ch)	DDR3 1600	426Ball FBGA (Lead & Halogen Free)



Ball ASSIGNMENT

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	
A	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD2	VDD1	VSS	VDD2	VDD1	VSS	VDDCA	VSS	VDD2	VSS	VDDCA	VSS	VDD2	VSS	VDDCA	VSS	VDDCA	VDD2	VDD1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	A
B	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DDR0_CA[1]	DDR0_CA[3]	DDR0_CSN[0]	DDR0_CKE[0]	VDD1	DDR0_CKB	DDR0_VREF_CA	DDR0_CA[6]	DDR0_CA[8]	DDR0_CA[9]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	B
C	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DDR0_CA[0]	DDR0_CA[2]	DDR0_CA[4]	DDR0_CSN[1]	DDR0_CKE[1]	DDR0_CK	VSS	DDR0_CA[5]	DDR0_CA[7]	DDR0_RREF_CA	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	C
D	VSS	VSS	VSS																																VSS	VSS	VDD1	D
E	VSS	VSS	VSS																																VSS	VSS	VDD2	E
F	VSS	VSS	VSS																																DDR1_DQ[30]	DDR1_DQ[31]	VSS	F
G	VSS	VSS	VSS																																DDR1_DQ[28]	DDR1_DQ[29]	VDDQ	G
H	VSS	VSS	VSS																																DDR1_DQ[26]	DDR1_DQ[27]	VSS	H
J	VDD2	VSS	VSS																																DDR1_DQ[24]	DDR1_DQ[25]	VDDQ	J
K	VDDCA	VSS	VSS																																DDR1_NDQS[3]	DDR1_PDQS[3]	VSS	K
L	VDD1	VSS	VSS																																DDR1_DM[3]	VDD2	VDDQ	L
M	VDD2	VSS	VSS																																DDR1_DQ[14]	DDR1_DQ[15]	VSS	M
N	VSS	DDR1_CA[9]	DDR1_RREF_CA																																DDR1_DQ[12]	DDR1_DQ[13]	VDDQ	N
P	VDDCA	DDR1_CA[8]	DDR1_CA[7]																																DDR1_DQ[10]	DDR1_DQ[11]	VSS	P
R	VSS	DDR1_CA[6]	DDR1_CA[5]																																DDR1_DQ[8]	DDR1_DQ[9]	VDDQ	R
T	VDD2	VSS	DDR1_VREF_CA																																DDR1_NDQS[1]	DDR1_PDQS[1]	VSS	T
U	VSS	DDR1_CKB	DDR1_CK																																VSS	DDR1_DM[1]	VDDQ	U
V	VDDCA	DDR1_CKE[1]	VDD1																																DDR1_VREF_DQ	VDD2	VDD1	V
W	VSS	DDR1_CKE[0]	DDR1_CSN[1]																																VSS	DDR1_DM[0]	VDDQ	W
Y	VDD2	DDR1_CSN[0]	DDR1_CA[4]																																DDR1_PDQS[0]	DDR1_NDQS[0]	VSS	Y
AA	VSS	DDR1_CA[3]	DDR1_CA[2]																																DDR1_DQ[6]	DDR1_DQ[7]	VDDQ	AA
AB	VDDCA	DDR1_CA[1]	DDR1_CA[0]																																DDR1_DQ[4]	DDR1_DQ[5]	VSS	AB
AC	VDD1	VSS	VSS																																DDR1_DQ[2]	DDR1_DQ[3]	VDDQ	AC
AD	VDD2	VSS	VSS																																DDR1_DQ[0]	DDR1_DQ[1]	VSS	AD
AE	VSS	VSS	VSS																																DDR1_DM[2]	VDD2	VDDQ	AE
AF	VSS	VSS	VSS																																DDR1_PDQS[2]	DDR1_NDQS[2]	VSS	AF
AG	VDD1	VSS	VSS																																DDR1_DQ[22]	DDR1_DQ[23]	VDDQ	AG
AH	VDD2	VSS	VSS																																DDR1_DQ[20]	DDR1_DQ[21]	VSS	AH
AJ	VSS	VSS	VSS																																DDR1_DQ[18]	DDR1_DQ[19]	VDDQ	AJ
AK	VSS	VSS	VSS																																DDR1_DQ[16]	DDR1_DQ[17]	VSS	AK
AL	VSS	VSS	VSS																																VSS	VSS	VDD2	AL
AM	VSS	VSS	VSS																																VSS	VSS	VDD1	AM
AN	VSS	VSS	VSS																																VSS	VSS	VSS	AN
AP	VSS	VSS	VSS																																VSS	VSS	VSS	AP
AR	VSS	VSS	VSS																																VSS	VSS	VSS	AR
AT	VSS	VSS	VSS																																VSS	VSS	VSS	AT
AU	VSS	VSS	VSS																																VSS	VSS	VSS	AU
AV	VSS	VSS	VSS	VSS	DDR0_DQ[17]	DDR0_DQ[19]	DDR0_DQ[21]	DDR0_DQ[23]	DDR0_NDQS[2]	DDR0_DM[2]	DDR0_DQ[1]	DDR0_DQ[3]	DDR0_DQ[5]	DDR0_DQ[7]	DDR0_NDQS[0]	VSS	DDR0_VREF_DQ	VSS	DDR0_PDQS[1]	DDR0_DQ[9]	DDR0_DQ[11]	DDR0_DQ[13]	DDR0_DQ[15]	DDR0_DM[3]	DDR0_PDQS[3]	DDR0_DQ[25]	DDR0_DQ[27]	DDR0_DQ[29]	DDR0_DQ[31]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AV
AW	VSS	VSS	VSS	VDDQ	DDR0_DQ[16]	DDR0_DQ[18]	DDR0_DQ[20]	DDR0_DQ[22]	DDR0_PDQS[2]	VDD2	DDR0_DQ[0]	DDR0_DQ[2]	DDR0_DQ[4]	DDR0_DQ[6]	DDR0_PDQS[0]	DDR0_DM[0]	VDD1	DDR0_DM[1]	DDR0_NDQS[1]	DDR0_DQ[8]	DDR0_DQ[10]	DDR0_DQ[12]	DDR0_DQ[14]	VDD2	DDR0_NDQS[3]	DDR0_DQ[24]	DDR0_DQ[26]	DDR0_DQ[28]	DDR0_DQ[30]	VDDQ	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AW
AY	VSS	VSS	VSS	VDD1	VDD2	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VDD2	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VSS	VDDQ	VDD2	VDD1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AY
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	

Pin Description

SYMBOL	DESCRIPTION	Type
CS0_n, CS1_n	Chip Select	Input
CK_c, CK_t	Differential Clocks	Input
CKE0, CKE1	Clock Enable	Input
CA0 ~ CA9	Command / Address	Input
DQ0 ~ DQ31	Data I/O	Input/Output
DM0 ~ DM3	Input Data Mask	Input/Output
DQS0_t ~ DQS3_t	Differential Data Strobe (rising edge)	Input/Output
DQS0_c ~ DQS3_c	Differential Data Strobe (falling edge)	Input/Output
ZQ	Drive Strength Calibration	Input/Output
VDD1	Core Power Supply	Power
VDD2	Core Power Supply	Power
VSS	Ground	Ground
VDDQ	I/O Power Supply	Power
VDDCA	CA Power Supply	Power
VSSCA	CA Ground	Ground
VSSQ	I/O Ground	Ground
VREF	Reference Voltage	Power

Input/Output Capacitance

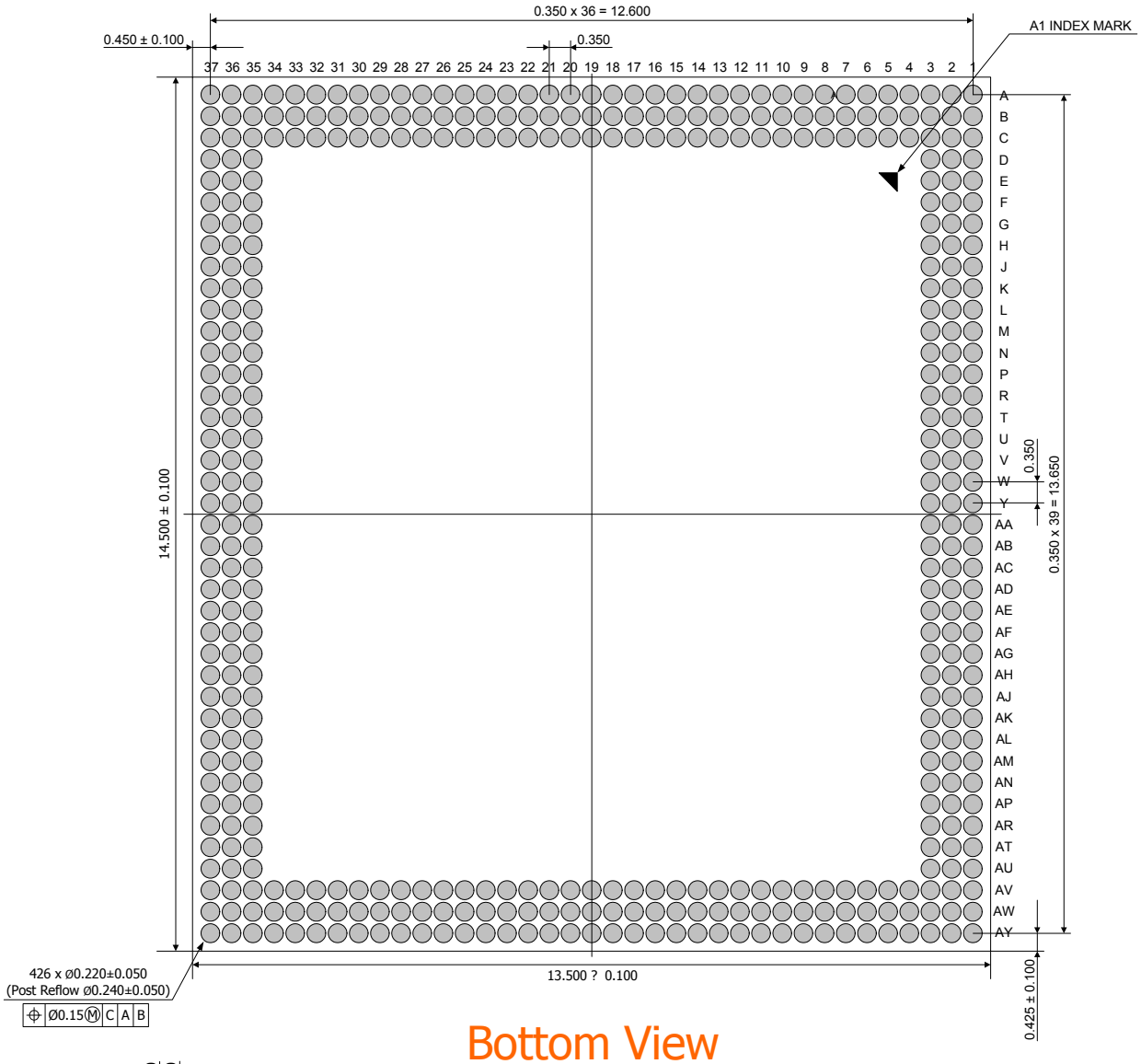
Parameter	Symbol	Min	Max	Unit
Input capacitance, CK_t and CK_c	CCK	TBD	TBD	pF
Input capacitance, all other input-only pins	CI	TBD	TBD	pF
Input/output capacitance, DQ, DM, DQS_t, DQS_c	CIO	TBD	TBD	pF
Input/Output Capacitance ZQ	CZQ	TBD	TBD	pF

(TOPER; VDDQ = 1.14-1.3V; VDDCA = 1.14-1.3V; VDD1 = 1.7-1.95V, VDD2 = 1.14-1.3V)

Note:
1. This parameter applies to both die and package.
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSCA, VSSQ applied and all other pins floating).
3. CI applies to CS_n, CKE, CA0-CA9.
4. DM loading matches DQ and DQS.
5. MR3 I/O configuration DS OP3-OP0 = 0001B (34.3 Ohm typical)
6. Maximum external load capacitance on ZQ pin, including packaging, board, pin, resistor, and other LPDDR3 devices: 5pF.

PACKAGE INFORMATION

426 Ball 0.35mm pitch 13.5mm x 14.5mm FBGA *[t = 0.64mm max]*



4Gb LPDDR3 SDRAM
B - Die

Input/Output Functional Description

SYMBOL	TYPE	DESCRIPTION
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. CKE is sampled at the positive Clock edge.
CS_n	Input	**Chip Select:** CS_n is considered part of the command code.CS_n is sampled at the positive Clock edge.
CA0 - CA9	Input	**DDR Command/Address Inputs:** Uni-directional command/address bus inputs. CA is considered part of the command code.
DQ0 - DQ15 (x16) DQ0 - DQ31 (x32)	I/O	**Data Input/Output:** Bi-directional data bus
DQS0_t, DQS1_t, DQS0_c, DQS1_c (x16) DQS0_t - DQS3_t, DQS0_c - DQS3_c (x32)	I/O	**Data Strobe (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data. For x16, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7; DQS1_t and DQS1_c to the data on DQ8 - DQ15. For x32 DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7, DQS1_t and DQS1_c to the data on DQ8 - DQ15, DQS2_t and DQS2_c to the data on DQ16 - DQ23, DQS3_t and DQS3_c to the data on DQ24 - DQ31.
DM0-DM1 (x16) DM0-DM3 (x32)	Input	**Input Data Mask:** DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS_t. Although DM is for input only, the DM loading shall match the DQ and DQS_t (or DQS_c). For x16 and x32 devices, DM0 is the input data mask signal for the data on DQ0-7. DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.
VDD1	Supply	**Core Power Supply 1**
VDD2	Supply	**Core Power Supply 2**
VDDCA	Supply	**Input Receiver Power Supply**: Power for CA0-9, CKE, CS_n, CK_t and CK_c input buffers.
VDDQ	Supply	**I/O Power Supply**: Power supply for data input/output buffers.
VREFCA	Supply	**Reference Voltage for CA Command and Control Input Receiver**: Reference voltage for all CA0-9, CKE, CS_n, CK_t and CK_c input buffers.
VREFDQ	Supply	**Reference Voltage for DQ Input Receiver**: Reference voltage for all Data input buffers.
VSS	Supply	**Ground**
VSSCA	Supply	**Ground for Input Receivers**
VSSQ	Supply	**I/O Ground**: Ground for data input/output buffers
ZQ	I/O	**Reference Pin for Output Drive Strength Calibration**

Functional Description

LPDDR3-SDRAM is a high-speed synchronous DRAM device internally configured as an 8-bank memory.

These devices contain the following number of bits:
4 Gb has 4,294,967,296 bits

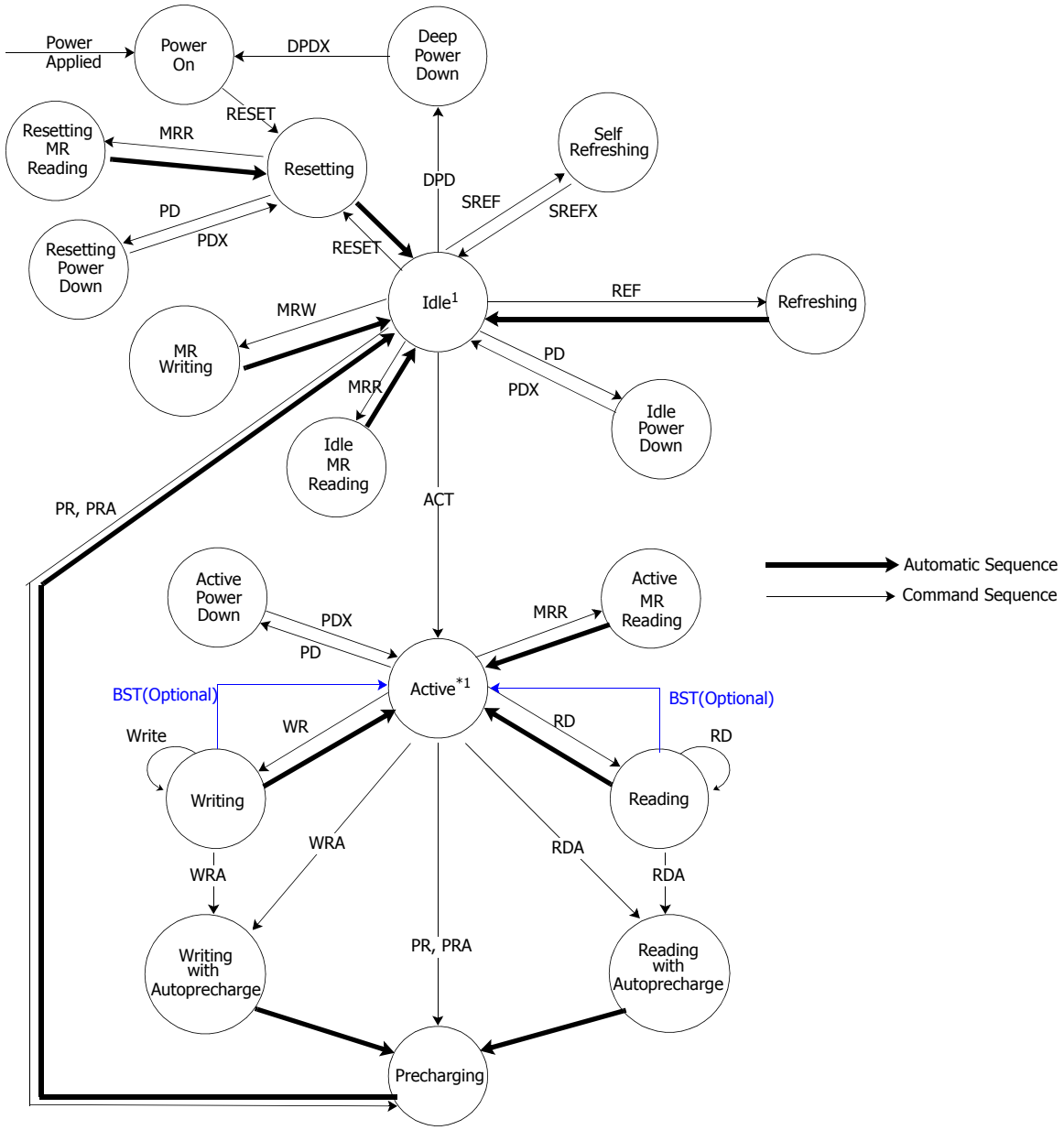
LPDDR3 devices use a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.
These devices also use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an 8n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR3 SDRAM effectively consists of a single 8n-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.
Read and write accesses to the LPDDR3 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.
Prior to normal operation, the LPDDR3 SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

LPDDR3 SDRAM Addressing

Density		4Gb
Number of Banks		8
Bank Addresses		BA0 - BA2
t_{REFI}(us)		3.9
x16	Row Addresses	R0 - R13
	Column Addresses	C0 - C10
x32	Row Addresses	R0 - R13
	Column Addresses	C0 - C9

Note:
1. The least-significant column address C0, C1 is not transmitted on the CA bus, and is implied to be zero.
2. tREFI values for all bank refresh is Tc = -30 ~ 85 °C, Tc means Operating Case Temperature.
3. Row and Column Address values on the CA bus which are not used are "don't care".

STATE DIAGRAM



PR(A) = Precharge (All)
ACT = Activate
WR(A) = Write (with Autoprecharge)
RD(A) = Read (with Autoprecharge)
BST(optional) = Burst Terminate
RESET = Reset is achieved through MRW command
MRW = Mode Register Write
MRR = Mode Register Read

PD = Enter Power Down
PDX = Exit Power Down
SREF = Enter Self Refresh
SREFX = Exit Self Refresh
DPD = Enter Deep Power Down
DPDX = Exit Deep Power Down
REF = Refresh

Note:
1. In the Idle state, all banks are precharged.
2. In the case of MRW to enter CA Training mode or Write Leveling Mode, the state machine will not automatically return to the Idle state. In these cases an additional MRW command is required to exit either operating mode and return to the Idle state. See sections "CA Training" or "Write Leveling".
3. The Operation “Burst Terminate” is supoprted as an optional feature.
4. Use caution with this diagram. It is intended to provide a floorplan of the possible state transitions and commands to control them, not all details. In particular, situations involving more than one bank are not captured in full detail.

Power-up, Initialization and Power-off

Voltage Ramp and Device Initialization

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory.

1. Voltage Ramp

While applying power (after Ta), CKE must be held LOW (≤ 0.2 × VDDCA), and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW.

Following the completion of the voltage ramp (Tb), CKE must be maintained LOW. DQ, DM, DQS_t and DQS_c voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latchup. CK_t, CK_c, CS_n, and CA input levels must be between VSSCA and VDDCA during voltage ramp to avoid latch-up. Voltage ramp power supply requirements are provided in the table "Voltage Ramp Conditions".

Table. Voltage Ramp Conditions

After...	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2-200mV.
	VDD1 and VDD2 must be greater than VDDCA-200mV.
	VDD1 and VDD2 must be greater than VDDQ-200mV.
	VREF must always be less than all other supply voltages.

Note:
1. Ta is the point when any power supply first reaches 300mV.
2. Noted conditions apply between Ta and power-off (controlled or uncontrolled).
3. Tb is the point at which all supply and reference voltages are within their defined operating ranges.
4. Power ramp duration tINIT0 (Tb - Ta) must not exceed 20ms.
5. The voltage difference between any of VSS, VSSQ, and VSSCA pins must not exceed 100mV.

Beginning at Tb, CKE must remain LOW for at least tINIT1, after which CKE can be asserted HIGH. The clock must be stable at least tINIT2 prior to the first CKE LOW-to-HIGH transition (Tc). CKE, CS_n, and CA inputs must observe setup and hold requirements (tIS, tIH) with respect to the first rising clock edge (as well as to subsequent falling and rising edges).

If any MRR commands are issued, the clock period must be within the range defined for tCKb. MRW commands can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least tINIT3 (Td).

2. Reset Command

After tINIT3 is satisfied, the MRW RESET command must be issued (Td).

An optional PRECHARGE ALL command can be issued prior to the MRW RESET command. Wait at least tINIT4 while keeping CKE asserted and issuing NOP commands. Only NOP commands are allowed during time tINIT4.

3. MRRs and Device Auto Initialization (DAI) Polling

After tINIT4 is satisfied (Te), only MRR commands and power-down entry/exit commands are supported. After Te, CKE can go LOW in alignment with power-down entry and exit specifications. MRR commands are only valid at this time if the CA bus does not need to be trained. may only begin after time Tf. User may issue MRR command to poll the DAI bit which will indicate if device auto initialization is complete; once DAI bit indicates completion, SDRAM is in idle state. Device will also be in idle state after tINIT5(max) has expired (whether or not DAI bit has been read by MRR command). As the memory output buffers are not properly configured by Te, some AC parameters must have relaxed timings before the system is appropriately configured.

After the DAI bit (MR0, DAI) is set to zero by the memory device (DAI complete), the device is in the idle state (Tf). DAI status can be determined by issuing the MRR command to MR0. The device sets the DAI bit no later than tINIT5 after the RESET command. The controller must wait at least tINIT5 or until the DAI bit is set before proceeding.

4. ZQ Calibration

If CA Training is not required, the MRW initialization calibration (ZQ_CAL) command can be issued to the memory (MR10) after time Tf. If CA Training is required, the CA Training may begin at time Tf. See the section of "Mode Register Write - CA Training Mode" for the CA Training command. No other CA commands (other than RESET or NOP) may be issued prior to the completion of CA Training. At the completion of CA Training (Tf'), the MRW initialization calibration (ZQ_CAL) command can be issued to the memory (MR10).

This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one LPDDR3 device exists on the same bus, the controller must not overlap MRW ZQ_CAL commands. The device is ready for normal operation after tZQINIT.

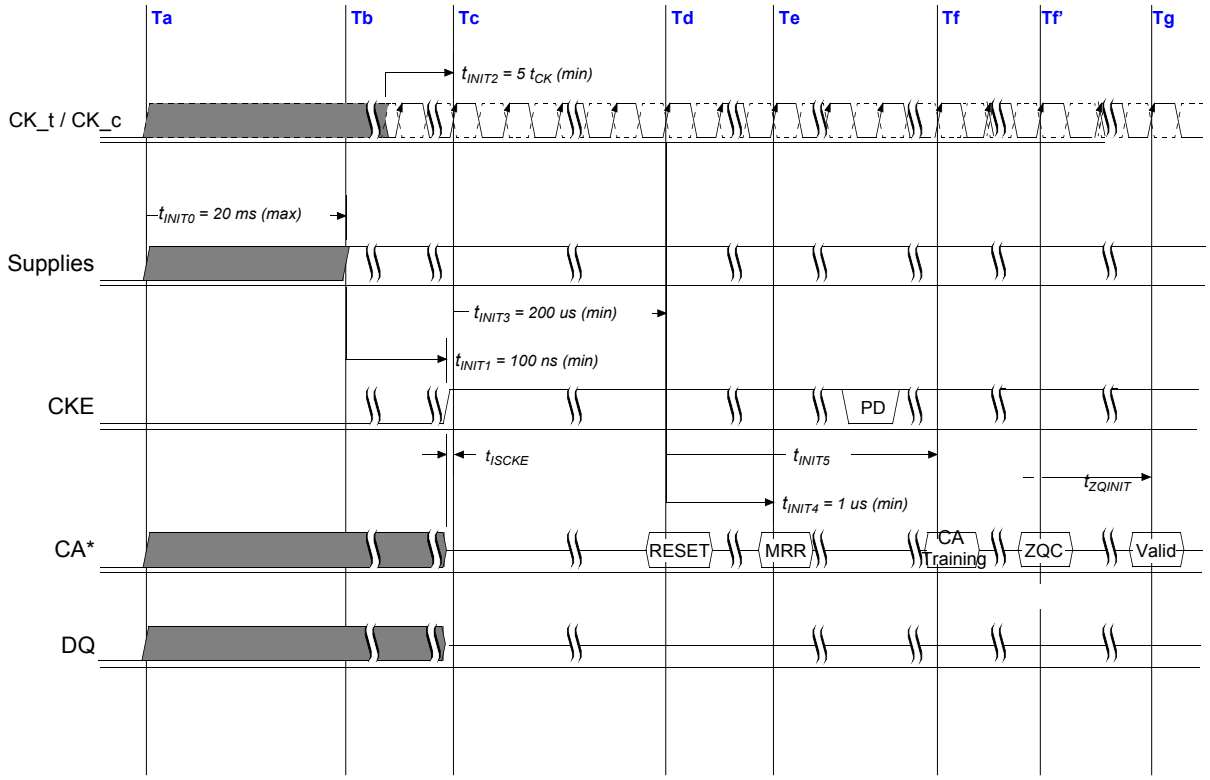
5. Normal Operation

After tZQINIT (Tg), MRW commands must be used to properly configure the memory (for example the output buffer drive strength, latencies, etc.). Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration.

After the initialization sequence is complete, the device is ready for any valid command. After Tg, the clock frequency can be changed using the procedure described in the LPDDR3 specification.

Table. Timing Parameters for initialization

Symbol	Parameter	Value		Unit
		min	max	
tINIT0	Maximum Voltage Ramp Time	-	20	ms
tINIT1	Minimum CKE low time after completion of voltage ramp	100	-	ns
tINIT2	Minimum stable clock before first CKE high	5	-	tCK
tINIT3	Minimum idle time after first CKE assertion	200	-	us
tINIT4	Minimum idle time after Reset command	1	-	us
tINIT5	Maximum duration of Device Auto-Initialization	-	10	us
tZQINIT	ZQ Initial Calibration for LPDDR3 devices	1	-	us
tCKb	Clock cycle time during boot	18	100	ns



* Midlevel on CA bus means: valid NOP

Figure. Power Ramp and Initialization Sequence

Notes
1. High-Z on the CA bus indicates NOP.
2. For tINIT values, see the table "Timing Parameters for Initialization".
3. CA Training is optional.

Initialization After Reset (without Power ramp)

If the RESET command is issued before or after the power-up initialization sequence, the re-initialization procedure must begin at Td.

Power-off Sequence

The following procedure is required to power off the device.
While powering off, CKE must be held LOW (≤ 0.2 × VDDCA); all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW.
DQ, DM, DQS_t, and DQS_c voltage levels must be between VSSQ and VDDQ during the power-off sequence to avoid latch-up. CK_t, CK_c, CS_n, and CA input levels must be between VSSCA and VDDCA during the power-off sequence to avoid latch-up.
Tx is the point where any power supply drops below the minimum value specified.
Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off (see the table "Power Supply Conditions").

Table. Power Supply Conditions

Between...	Applicable Conditions
Tx and Tz	VDD1 must be greater than VDD2—200mV
	VDD1 must be greater than VDDCA—200mV
	VDD1 must be greater than VDDQ—200mV
	VREF must always be less than all other supply voltages

The voltage difference between any of VSS, VSSQ, and VSSCA pins must not exceed 100mV.

Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:
At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.
After Tz (the point at which all power supplies first reach 300mV), the device must power off. The time between Tx and Tz must not exceed 10ms. During this period, the relative voltage between power supplies is uncontrolled. VDD1 and VDD2 must decrease with a slope lower than 0.5 V/µs between Tx and Tz.
An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table. Power-Off Timing

Symbol	Parameter	Value		Unit
		min	max	
tPOFF	Maximum power-off ramp time	-	2	sec

Mode Register Definition

Table below shows the mode registers for LPDDR3 SDRAM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command shall be used to read a mode register. A Mode Register Write command shall be used to write a mode register.

Table. Mode Register Assignment

MR #	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00H	Device Info.	R	RL3	WL set B	(RFU)	RZQI (Optional)		(RFU)		DAI	go to MR0
1	01H	Device Feature1	W	nWR (for AP)			(RFU)	BT	BL			go to MR1
2	02H	Device Feature 2	W	WR Lev	WL Select	(RFU)	nWRE	RL & WL				go to MR2
3	03H	I/O Config-1	W	(RFU)				DS				go to MR3
4	04H	Device Tempera-ture	R	TUF	(RFU)			Refresh Rate				go to MR4
5	05H	Basic Config-1	R	Manufacturer ID								go to MR5
6	06H	Basic Config-2	R	Revision ID1								go to MR6
7	07H	Basic Config-3	R	Revision ID2								go to MR7
8	08H	Basic Config-4	R	I/O width		Density				Type		go to MR8
9	09H	Test Mode	W	Vendor-Specific Test Mode								go to MR9
10	0AH	Calibration	W	Calibration Code								go to MR10
16	10H	PASR_Bank	W	PASR Bank Mask								go to MR16
17	11H	PASR_Segment	W	PASR Segment Mask								go to MR17
32	20H	DQ Calibration Pattern A	R	See the section "DQ Calibration"								go to MR32
40	28H	DQ Calibration Pattern B	R	See the section "DQ Calibration"								go to MR40
41	29H	CA Training Entry for CA0-3, CA5-8	W	See the section "Mode Register Write - CA Training Mode"								go to MR41
42	2AH	CA Training Exit	W	See the section "Mode Register Write - CA Training Mode"								go to MR42
48	30H	CA Training Entry for CA4, 9	W	See the section "Mode Register Write - CA Training Mode"								go to MR48
63	3FH	Reset	W	X								go to MR63

Note:
1. RFU bits shall be set to `0' during Mode Register writes.
2. RFU bits shall be read as `0' during Mode Register reads.
3. All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS_t, DQS_c shall be toggled.
4. All Mode Registers that are specified as RFU shall not be written.
5. Writes to read-only registers shall have no impacts on the functionality of the device.

MR0 Device Information (MA<7:0> = 00H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RL3	WL (Set B) Support	(RFU)	RZQI (Optional)		(RFU)		DAI

DAI (Device Auto-Initialization Status)	Read-only	OP0	0B: DAI complete 1B: DAI still in progress
RZQI (Built in Self Test for RZQ Information)	Read-only	OP4:OP3	00B: RZQ self test not supported 01B: ZQ-pin may connect to VDDCA or float 10B: ZQ-pin may short to GND 11B: ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDD or float nor short to GND)
WL (Set B) Support	Read-only	OP<6>	0B: DRAM does not support WL (Set B) 1B: DRAM supports WL (Set B)
RL3 Option Support	Read-only	OP<7>	0B : DRAM does not support RL=3, nWR=3, WL=1 1B : DRAM supports RL=3, nWR=3, WL=1 for frequencies <=166

Note:
1. RZQI, if supported, will be set upon completion of the MRW ZQ Initialization Calibration command.
2. If ZQ is connected to VDDCA to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDDCA, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3. In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per Note 4), the LPDDR3 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
4. In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240-ohm +/-1%).

MR1 Device Feature 1 (MA<7:0> = 01H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			(RFU)	BT	BL		

BL	Write-only	OP<2:0>	011B: BL8 (default)
			100B: BL16 (optional)
			All others: reserved
BT	Write-only	OP<3>	0B: Don't care
nWR	Write-only	OP<7:5>	If nWRE (in MR2 OP4) = 0
			001B : nWR=3 (optional)
			100B : nWR=6
			110B : nWR=8
			111B : nWR=9
			If nWRE (in MR2 OP4) = 1
			000B : nWR=10 (default)
			001B : nWR=11
			010B : nWR=12
			100B : nWR=14
			110B : nWR=16
			All others: reserved

Note:
1. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

Table. Burst Sequence by BL and BT

C3	C2	C1	C0	BT	BL	Burst Cycle Number and Burst Address Sequence															
						1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
X	0B	0B	0B	seq	8	0	1	2	3	4	5	6	7								
X	0B	1B	0B			2	3	4	5	6	7	0	1								
X	1B	0B	0B			4	5	6	7	0	1	2	3								
X	1B	1B	0B			6	7	0	1	2	3	4	5								
X	X	X	0B	int		illegal (not allowed)															
X	X	X	0B	seq	16	illegal (not allowed)															
0B	0B	0B	0B	int		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0B	1B	0B	0B			4	5	6	7	0	1	2	3	C	D	E	F	8	9	A	B
1B	0B	0B	0B			8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1B	1B	0B	0B			C	D	E	F	8	9	A	B	4	5	6	7	0	1	2	3

Note:
1. C0 inputs are not present on CA bus. Those are implied zero.
2. For BL=8, the burst address represents C2 - C0.
3. For BL=16, the burst address represents C3 - C0.
4. 'seq' means sequential and 'int' means interleaved.

MR2 Device Feature 2 (MA<7:0> = 02H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WR Lev	WL Select	(RFU)	nWRE	RL & WL			

RL & WL	Write-only	OP<3:0>	If OP<6> =0 (WL Set A, default) 0001B: RL = 3 / WL = 1 (≤ 166 MHz, optional[1]) 0100B: RL = 6 / WL = 3 (≤ 400 MHz) 0110B: RL = 8 / WL = 4 (≤ 533 MHz) 0111B: RL = 9 / WL = 5 (≤ 600 MHz) 1000B: RL = 10 / WL = 6 (≤ 667 MHz, default) 1001B: RL = 11 / WL = 6 (≤ 733 MHz) 1010B: RL = 12 / WL = 6 (≤ 800 MHz) 1100B: RL = 14 / WL = 8 (≤ 933 MHz) 1110B: RL = 16 / WL = 8 (≤ 1066 MHz) All others: reserved If OP<6> =1 (WL Set B, optional[2]) 0001B: RL = 3 / WL = 1 (≤ 166 MHz, optional[1]) 0100B: RL = 6 / WL = 3 (≤ 400 MHz) 0110B: RL = 8 / WL = 4 (≤ 533 MHz) 0111B: RL = 9 / WL = 5 (≤ 600 MHz) 1000B: RL = 10 / WL = 8 (≤ 667 MHz, default) 1001B: RL = 11 / WL = 9 (≤ 733 MHz) 1010B: RL = 12 / WL = 9 (≤ 800 MHz) 1100B: RL = 14 / WL = 11 (≤ 933MHz) 1110B: RL = 16 / WL = 13 (≤ 1066MHz) All others: reserved
nWRE	Write-only	OP<4>	0B : Enable nWR programing ≤ 9
			1B : Enable nWR programing > 9 (default)
WL Select	Write-only	OP<6>	0B : Select WL Set A (default)
			1B : Select WL Set B (optional[2])
Write Leveling	Write-only	OP<7>	0B : Disabled (default)
			1B : Enabled

Note:
1. See MR0, OP<7>.
2. See MR0, OP<6>.

MR3 I/O Configuration 1 (MA<7:0> = 03H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

DS	Write-only	OP<3:0>	0000B: reserved
			0001B: 34.3Ω typical pull-down/pull-up
			0010B: 40Ω typical pull-down/pull-up (default)
			0011B: 48Ω typical pull-down/pull-up
			0100B: reserved for 60Ω typical pull-down/pull-up
			0110B: reserved for 80Ω typical pull-down/pull-up
			1001B: 34.3Ω typical pull-down, 40Ω Typical Pull-up (optional[1])
			1010B: 40Ω typical pull-down, 48Ω Typical Pull-up (optional[1])
			1011B: 34.3Ω typical pull-down, 48Ω Typical Pull-up (optional[1])
			All others: reserved

Note:
1. Please contact us, for the supportability of the optional feature.

MR4 Device Temperature (MA<7:0> = 04H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				Refresh Rate		

Refresh Rate	Read-only	OP<2:0>	000B: Low temperature operating limit exceeded
			001B: 4 x tREFI, 4 x tREFIpb, 4 x tREFW (≤ 35°C)
			010B: 2 x tREFI, 2 x tREFIpb, 2 x tREFW (36 - 60°C)
			011B: 1 x tREFI, 1 x tREFIpb, 1 x tREFW (61 - 85°C)
			100B: 1/2 x tREFI, 1/2 x tREFIpb, 1/2 x tREFW, do not de-rate AC timing (86 - 90°C)
			101B: 1/4 x tREFI, 1/4 x tREFIpb, 1/4 x tREFW, do not de-rate AC timing (91 - 95°C)
			110B: 1/4 x tREFI, 1/4 x tREFIpb, 1/4 x tREFW, de-rate AC timing (96 - 105°C)
			111B: High temperature operating limit exceeded (> 105°C)
Temperature Update Flag (TUF)	Read-only	OP<7>	0B: OP<2:0> value has not changed since last read of MR4 1B: OP<2:0> value has changed since last read of MR4

Note:
1. A Mode Register Read from MR4 will reset OP7 to '0'.
2. OP7 is reset to '0' at power-up.
3. If OP2 equals '1', the device temperature is greater than 85°C.
4. OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.
5. LPDDR3 might not operate properly when OP[2:0] = 000B or 111B.
6. For specified operating temperature range and maximum operating temperature refer to the section of Operating Temperature Range.
7. LPDDR3 devices shall be de-rated by adding derating values to the following core timing parameters: tRCD, tRC, tRAS, tRP and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating in "AC timing table". Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.
8. See the section of Temperature Sensor for information on the recommended frequency of reading MR4.

MR5 Basic Configuration1 (MA<7:0> = 05H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Manufacturer ID							

Company ID	Read-only	OP<7:0>	0000 0110B: Hynix Semiconductor	

MR6 Basic Configuration2 (MA<7:0> = 06H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID 1							

Revision ID1	Read-only	OP<7:0>	00000000B: A-version	

MR7 Basic Configuration3 (MA<7:0> = 07H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID 2							

Revision ID2	Read-only	OP<7:0>	00000000B: A-version	

MR8 Basic Configuration4 (MA<7:0> = 08H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Type	Read-only	OP<1:0>	11B: S8
			All Others : Reserved
Density	Read-only	OP<5:2>	0110B : 4Gb
			1110B : 6Gb
			0111B : 8Gb
			1101B : 12Gb
			1000B : 16Gb
			All Others : Reserved
I/O width	Read-only	OP<7:6>	00B: x32
			01B: x16
			All Others : Reserved

MR9 Test Mode (MA<7:0> = 09H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific Test Mode							

MR10 Calibration (MA<7:0> = 0AH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write Only	OP<7:0>	1111 1111B: Calibration command after initialization
			1010 1011B: Long Calibration
			0101 0110B: Short Calibration
			1100 0011B: ZQ Reset
			others: reserved

Note:
1. Host processor shall not write MR10 with "Reserved" values
2. LPDDR3 devices shall ignore calibration command when a "Reserved" value is written into MR10.
3. See AC timing table for the calibration latency.
4. If ZQ is connected to VSSCA through RZQ, either the ZQ calibration function (see "Mode Register Write ZQ Calibration Command") or default calibration (through the ZQRESET command) is supported. If ZQ is connected to VDDCA, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.
5. LPDDR3 devices that do not support calibration shall ignore the ZQ Calibration command.
6. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

MR11:15 (Reserved) (MA<7:0> = 0CH - 0FH)

MR16 PASR Bank Mask (MA<7:0> = 10H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank Mask							

Bank <7:0> Mask	Write-only	OP<7:0>	0B : refresh enable to the bank (=unmasked, default) 1B : refresh blocked (=masked)

OP	Bank Mask	LPDDR3 SDRAM
0	XXXXXXX1	Bank 0
1	XXXXXX1X	Bank 1
2	XXXXX1XX	Bank 2
3	XXXX1XXX	Bank 3
4	XXX1XXXX	Bank 4
5	XX1XXXXX	Bank 5
6	X1XXXXXX	Bank 6
7	1XXXXXXX	Bank 7

MR17 PASR Segment Mask (MA<7:0> = 11H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

Segment <7:0> Mask	Write-only	OP<7:0>	0B : refresh enable to the segment (=unmasked, default) 1B : refresh blocked (=masked)

Segment	OP	Segment Mask	4Gb R13:11	6Gb[2] R14:12	8Gb R14:12	12Gb[2] R14:12	16Gb R14:12
0	0	XXXXXXX1	000B				
1	1	XXXXXX1X	001B				
2	2	XXXXX1XX	010B				
3	3	XXXX1XXX	011B				
4	4	XXX1XXXX	100B				
5	5	XX1XXXXX	101B				
6	6	X1XXXXXX	110B				
7	7	1XXXXXXX	111B				

Note:
1. This table indicates the range of row addresses in each masked segment. X is do not care for a particular segment.
2. No memory present at addresses with R13=R14=HIGH. Segment masks 6 and 7 are ignored.

MR18:31 (Reserved) (MA<7:0> = 12H - 1FH)

MR32 DQ Calibration Pattern A (MA<7:0> = 20H): MRR only
Reads to MR32 return DQ Calibration Pattern A. See the section "DQ Calibration".

MR33:39 (Reserved) (MA<7:0> = 21H - 27H)

MR40 DQ Calibration Pattern B (MA<7:0> = 28H): MRR only
Reads to MR40 return DQ Calibration Pattern B. See the section "DQ Calibration".

MR41 CA Calibration Mode Entry for CA0-3, CA5-8 (MA<7:0> = 29H)
Write to MR41 enables CA Training. See the section "Mode Register Write - CA Training Mode".

MR42 CA Calibration Mode Exit (MA<7:0> = 2AH)
Write to MR42 exits CA Training. See the section "Mode Register Write - CA Training Mode".

MR43:47 (Reserved) (MA<7:0> = 2BH - 2FH)

MR48 CA Calibration Mode Entry for CA4, 9 (MA<7:0> = 30H)
Write to MR48 enables CA Training. See the section "Mode Register Write - CA Training Mode".

MR49:62 (Reserved) (MA<7:0> = 31H - 3EH)

MR63 Reset (MA<7:0> = 3FH): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X or 0xFC							

Note: For additional information on MRW RESET, see Mode Register Write Command section.

TRUTH TABLES

Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the LPDDR3 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

COMMAND TRUTH TABLE

Command	SDR Command Pins (2)			DDR CA Pins (10)										CK_t edge
	CKE		CS_n	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
	CK_t(n-1)	CK_t(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	rising
			X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	falling
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	rising
			X	MA6	MA7	X								falling
Refresh (per bank)	H	H	L	L	L	H	L	X						rising
			X	X										falling
Refresh (all bank)	H	H	L	L	L	H	H	X						rising
			X	X										falling
Enter Self Refresh	H	L	L	L	L	H	X							rising
			X	X										falling
Active (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	rising
			X	R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	falling
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	rising
			X	AP[3]	C3	C4	C5	C6	C7	C8	C9	C10	C11	falling
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	rising
			X	AP[3]	C3	C4	C5	C6	C7	C8	C9	C10	C11	falling
Precharge (per bank, all bank)[11]	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	BA2	rising
			X	X	X	X	X	X	X	X	X	X	X	falling
BST (optional)	H	H	L	H	H	L	L	X						rising
			X	X										falling
Enter Deep Power Down	H	L	L	H	H	L	X							rising
			X	X										falling
NOP	H	H	L	H	H	H	X							rising
			X	X										falling
Maintain SREF, PD, DPD (NOP)[4]	L	L	L	H	H	H	X							rising
			X	X										falling
NOP	H	H	H	X										rising
			X	X										falling
Maintain PD, SREF, DPD (NOP)[4]	L	L	X	X										rising
			X	X										falling
Enter Power Down	H	L	H	X										rising
			X	X										falling
Exit PD, SREF, DPD	L	H	H	X										rising
			X	X										falling

Note:

1. All LPDDR3 commands are defined by states of CS_n, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2. Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.
3. AP "high" during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.
4. "X" means "H or L (but a defined logic level)", except when the LPDDR3 SDRAM is in PD, SREF, or DPD, in which case CS_n, CK_t/CK_c, and CA can be floated after the required tCPDED time is satisfied, and until the required exit procedure is initiated as described in the respective entry/exit procedure.
5. Self refresh exit and Deep Power Down exit are asynchronous.
6. VREF must be between 0 and VDDQ during Self Refresh and Deep Power Down operation.
7. CAxr refers to command/address bit "x" on the rising edge of clock.
8. CAxf refers to command/address bit "x" on the falling edge of clock.
9. CS_n and CKE are sampled at the rising edge of clock.
10. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
11. AB "high"during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is do-not-care.
12. When CS_n is HIGH, LPDDR3 CA bus can be floated.

CKE TRUTH TABLE

Current State[3]	CKE_{n-1} [4]	CKE_n[4]	CS_n[5]	Command n[6]	Operation n[6]	Next State	Notes
Active Power Down	L	L	X	X	Maintain Active Power Down	Active Powe Down	
	L	H	H	NOP	Exit Active Power Down	Active	7
Idl Power Down	L	L	X	X	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	7
Resetting Power Down	L	L	X	X	Maintain Resetting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	7,10
Deep Power Down	L	L	X	X	Maintain Deep Power Down	Deep Power Down	
	L	H	H	NOP	Exit Deep Power Down	Power On	9
Self Refresh	L	L	X	X	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	8
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power-Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Down	
	H	L	L	Enter Self Refresh	Enter Self Refresh	Self Refresh	
	H	L	L	Deep Power Down	Enter Deep Power Down	Deep Power Down	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
	H	H	Refer to the Command Truth Table				

Note:
1. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
2. 'X' means 'Don't care'.
3. "Current state" is the state of the LPDDR3 device immediately prior to clock edge n.
4. "CKEn" is the logic state of CKE at clock rising edge n; "CKEn-1" was the state of CKE at the previous clock edge.
5. "CS_n" is the logic state of CS_n at the clock rising edge n.
6. "Command n" is the command registered at clock edge N, and "Operation n" is a result of "Command n".
7. Power Down exit time (tXP) should elapse before a command other than NOP is issued. The clock must toggle at least twice during the tXP period.
8. Self-Refresh exit time (tXSR) should elapse before a command other than NOP is issued. The clock must toggle at least twice during the tXSR time.
9. The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
10. Upon exiting Resetting Power Down, the device will return to the Idle state if tINIT5 has expired.

Current State Bank n - Command to Bank n

Current State	Command	Operation	Next State	Note
Any	NOP	Continue previous operation	Current State	
Idle	Activate	Select and activate row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Bank)	Begin to refresh	Refreshing (All Bank)	7
	MRW	Write value to Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	8
	Precharge	Deactive row in bank or banks	Precharging	9, 12
Row Active	Read	Select Column, and start read burst	Reading	
	Write	Select Column, and start write burst	Writing	
	MRR	Read value from Mode Register	Active MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading	Read	Select column, and start new read burst	Reading	10,11
	Write	Select column, and start write burst	Writing	10,11,13
	BST (optional)	Read burst terminate	Active	15
Writing	Write	Select Column, and start new write burst	Writing	10,11
	Read	Select column, and start read burst	Reading	10,11,14
	BST (optional)	Write burst terminate	Active	15
Power On	Reset	Begin Device Auto-Initialization	Resetting	7, 9
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Note:
1. The table applies when both CKE_{n-1} and CKE_n are HIGH, and after tXSR or tXP has been met if the previous state was Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State Definitions:
   Idle: The bank or banks have been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts / accesses and no register accesses are in progress.
   Reading: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Writing: A WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state and Table "Current State Bank n - Command to Bank n", and according to Table "Current State Bank n - Command to Bank m".
   Precharging: starts with the registration of a PRECHARGE command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
   Row Activating: starts with registration of an ACTIVE command and ends when tRCD is met. Once tRCD is met, the bank will be in the 'Active' state.
   Read with AP Enabled: starts with the registration of the READ command with Auto Precharge enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.
   Write with AP Enabled: starts with registration of a WRITE command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.
   Refreshing (Per Bank): starts with registration of a REFRESH (Per Bank) command and ends when tRFCpb is met. Once tRFCpb is met, the bank will be in an 'idle' state.
   Refreshing (All Bank): starts with registration of a REFRESH(All Bank) command and ends when tRFCab is met. Once tRFCab is met, the device will be in an 'all banks idle' state.
   Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
   Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.
   Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Row Active state.
   MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.
   Precharging All: starts with the registration of a PRECHARGE ALL command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
6. Bank-specific; requires that the bank is idle and no bursts are in progress.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. Not bank-specific reset command is achieved through MODE REGISTER WRITE command.
9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
10. A command other than NOP should not be issued to the same bank while a READ or WRITE burst with Auto Precharge is enabled.
11. The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
12. If a Precharge command is issued to a bank in the Idle state, tRP shall still apply.
13. A WRITE command may be applied after the completion of the READ burst; otherwise, a BST must be used to end the READ prior to asserting a WRITE command.
14. A READ command may be applied after the completion of the WRITE burst; otherwise, a BST must be used to end the WRITE prior to asserting a READ command.
15. Not bank-specific. BURST TERMINATE command affects the most recent read/write burst started by the most recent READ/WRITE command, regardless of bank.

Current State Bank n - Command to Bank m

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	Note
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	-	
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank m	Active	6
	Read	Select column, and start read burst from Bank m	Reading	7
	Write	Select column, and start write burst to Bank m	Writing	7
	Precharge	Deactivate row in bank or banks	Precharging	8
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	9,10,12
	BST (optional)	Read or Write burst terminate an ongoing Read/Write from/to Bank m	Active	
Reading (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	7
	Write	Select column, and start write burst to Bank m	Writing	7,15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Writing (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	7,16
	Write	Select column, and start write burst to Bank m	Writing	7
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Reading with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	7,13
	Write	Select column, and start write burst to Bank m	Writing	7,15,13
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Writing with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	7,13,16
	Write	Select column, and start write burst to Bank m	Writing	7,13
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Power On	Reset	Begin Device Auto-Initialization	Resetting	11, 14
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Note:
1. The table applies when both CKE_{n-1} and CKE_n are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State Definitions:
   Idle: the bank has been precharged, and tRP has been met.
   Active: a row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   Reading: a READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Writing: a WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4. REFRESH, SELF REFRESH, and MODE REGISTER WRITE commands may only be issued when all bank are idle.

5. The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:
   Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
   Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.
   Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Row Active state.
   MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.
6. tRRD must be met between Activate command to Bank n and a subsequent Activate command to Bank m.
7. READs or WRITEs listed in the Command column include READs and WRITEs with Auto Precharge enabled and READs and WRITEs with Auto Precharge disabled.
8. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
9. MRR is allowed during the Row Activating state and MRW is prohibited during the Row Activating state. (Row Activating starts with registration of an Activate command and ends when tRCD is met.)
10. MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when tRP is met.
11. Not bank-specific; requires that all banks are idle and no bursts are in progress.
12. The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon tRCD and tRP respectively.
13. Read with auto precharge enabled or a Write with auto precharge enabled may be followed by any valid command to other banks provided that the timing restrictions in the section of Precharge and Auto Precharge clarification are followed.
14. Reset command is achieved through MODE REGISTER WRITE command.
15. A WRITE command may be applied after the completion of the READ burst, otherwise a BST must be issued to end the READ prior to asserting a WRITE command.
16. A READ command may be applied after the completion of the WRITE burst; otherwise, a BST must be issued to end the WRITE prior to asserting a READ command.
17. BST is allowed only if a Read or Write burst is ongoing
18. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.

DATA MASK TRUTH TABLE

Function	DM	DQ	Note
Write Enable	L	Valid	1
Write Inhibit	H	X	1

Note:
1. Used to mask write data, provided coincident with the corresponding data.

Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Parameter	Symbol	Min	Max	Unit	Notes
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.3	V	1
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.6	V	1
VDDCA supply voltage relative to VSSCA	VDDCA	-0.4	1.6	V	1, 2
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.6	V	1, 3
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.4	1.6	V	
Storage Temperature	TSTG	-55	125	°C	4

Note:
1.See the section "Power-up, Initialization, and Power-off" for relationships between power supplies.
2. VREFCA ≤ 0.6 x VDDCA; however, VREFCA may be ≥ VDDCA provided that VREFCA ≤ 300mV.
3. VREFDQ ≤ 0.7 x VDDQ; however, VREFDQ may be ≥ VDDQ provided that VREFDQ ≤ 300mV.
4. Storage Temperature is the case surface temperature on the center/top side of the device. For the measurement conditions, please refer to JESD51-2 standard.

AC and DC Operating Conditions

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR3 Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Core Power 1	VDD1	1.70	1.80	1.95	V
Core Power 2	VDD2	1.14	1.20	1.30	V
Input Buffer Power	VDDCA	1.14	1.20	1.30	V
I/O Buffer Power	VDDQ	1.14	1.20	1.30	V

Note :
1. VDD1 uses significantly less current than VDD2.
2. The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 1MHz at the DRAM package ball.

Input Leakage Current

Parameter	Symbol	Min	Max	Unit	Note
Input Leakage current	IL	-2	2	uA	2
VREF supply leakage current	IVREF	-1	1	uA	1

Note:
1. For CA, CKE, CS_n, CK_t, CK_c. Any input 0V ≤ VIN ≤ VDDCA(All other pins not under test = 0V)
2. Although DM is for input only, the DM leakage shall match the DQ and DQS_t/DQS_c output leakage specification.
3. The minimum limit requirement is for testing purposes. The leakage current on VREFCA and VREFDQ pins should be minimal.
4. VREFDQ = VDDQ/2 or VREFCA = VDDCA/2. (All other pins not under test = 0V)

Operating Temperature

Parameter		Symbol	Min	Max	Unit	Note
Operating Temperature	Standard	T_{OPER}	-30	85	°C	1
	Extended		-30	105		1

Note:
1. Operating Temperature is the case surface temperature on the center-top side of the LPDDR3 device. For the measurement conditions, please refer to JESD51-2 standard.
2. Some applications require operation of LPDDR3 in the maximum temperature conditons in the Extended Temperature Range between -30°C and 105°C case temperature. For LPDDR3 devices, derating may be neccessary to operate in this range. See MR4 on the section "Mode Register".
3. Either the device case temperature rating or the temperature sensor (See the section of "Temperature Sensor") may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard or Elevated Temperature Ranges. For example, TCASE may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

AC and DC Input Measurement Levels

AC and DC Logic Input Levels for Single-Ended CA and CS_n Signals

Parameter	Symbol	LPDDR3 1600/1333		Unit	Note
		Min	Max		
AC Input Logic High	VIHCA	VREF + 0.150	Note 2	V	1,2
AC Input Logic Low	VILCA	Note 2	VREF - 0.150	V	1,2
DC Input Logic High	VIHCA	VREF + 0.100	VDDCA	V	1
DC Input Logic Low	VILCA	VSSCA	VREF - 0.100	V	1
Reference Voltage for CA and CS_n Inputs	VREFCA(DC)	0.49 * VDDCA	0.51 * VDDCA	V	3,4

Note:
1. For CA and CS_n input only pins. VREF = VREFCA(DC).
2. See the section "Overshoot and Undershoot Specifications".
3. The ac peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than +/-1% VDDCA (for reference: approx. +/- 12 mV).
4. For reference: approx. VDDCA/2 +/- 12 mV.

AC and DC Logic Input Levels for CKE

Parameter	Symbol	Min	Max	Unit	Note
CKE Input High Level	VIHCKE	0.65 * VDDCA	Note 1	V	1
CKE Input Low Level	VILCKE	Note 1	0.35 * VDDCA	V	1

Note: 1. See the section "Overshoot and Undershoot Specifications".

AC and DC Logic Input Levels for Single-Ended Data (DQ and DM) Signals

Parameter	Symbol	LPDDR3 1600/1333		Unit	Note
		Min	Max		
AC Input High Voltage	VIHDQ	VREF + 0.150	Note 2	V	1,2
AC Input Low Voltage	VILDQ	Note 2	VREF - 0.150	V	1,2
DC Input High Voltage	VIHDQ	VREF + 0.100	VDDQ	V	1
DC Input Low Voltage	VILDQ	VSSCA	VREF - 0.100	V	1
Reference Voltage for DQ and DM Inputs	VREFDQ(DC)	0.49 * VDDQ	0.51*VDDQ	V	3,4

Note:
1. For DQ input only pins. VREF = VREFDQ(DC).
2. See the section of Overshoot and Undershoot Specifications.
3. The ac peak noise on VREFDQ may not allow VREFDQ to deviate from VREFDQ(DC) by more than +/-1% VDDQ (for reference: approx. +/- 12 mV).
4. For reference: approx. VDDQ/2 +/- 12 mV.

VREF Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages VREFCA and VREFDQ are illustrated in Figure below. It shows a valid reference voltage VREF(t) as a function of time. (VREF stands for VREFCA and VREFDQ likewise). VDD stands for VDDCS for VREFCA and VDDQ for VREFDQ. VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g. 1 sec) and is specified as a fraction of the linear average of VDDCA or VDDQ also over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in Table "Electrical Characteristics and Operating Conditions". Furthermore VREF(t) may temporarily deviate from VREF(DC) by no more than +/- 1% VDD. VREF(t) cannot track noise on VDDQ or VDDCA if this would send VREF outside these specifications.

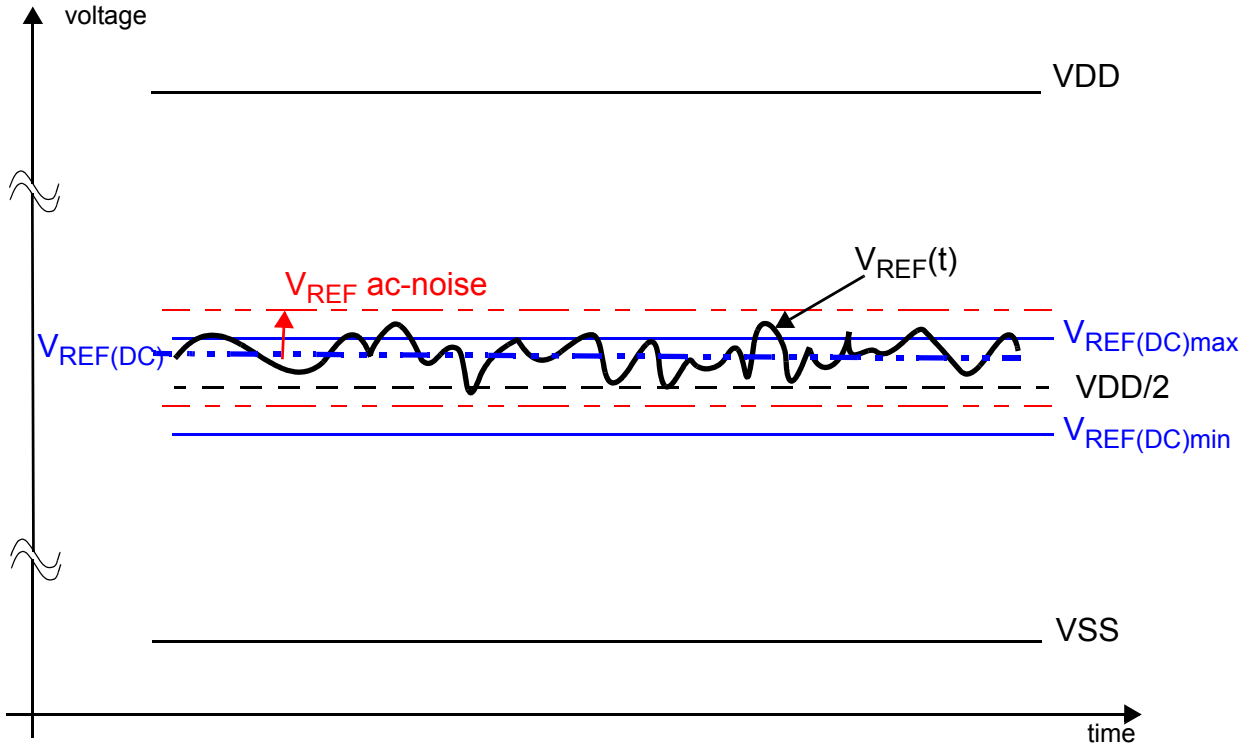


Figure. Illustration of VREF(DC) tolerance and VREF ac-noise limits

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREF. "VREF " shall be understood as VREF(DC), as defined in Figure above.

This clarifies that dc-variations of VRef affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VREF(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the LPDDR3 setup/hold specification and derating values need to include time and voltage associated with VREF ac-noise. Timing and voltage effects due to ac-noise on VREF up to the specified limit (+/-1% of VDD) are included in LPDDR3 timings and their associated deratings.

Input Signal

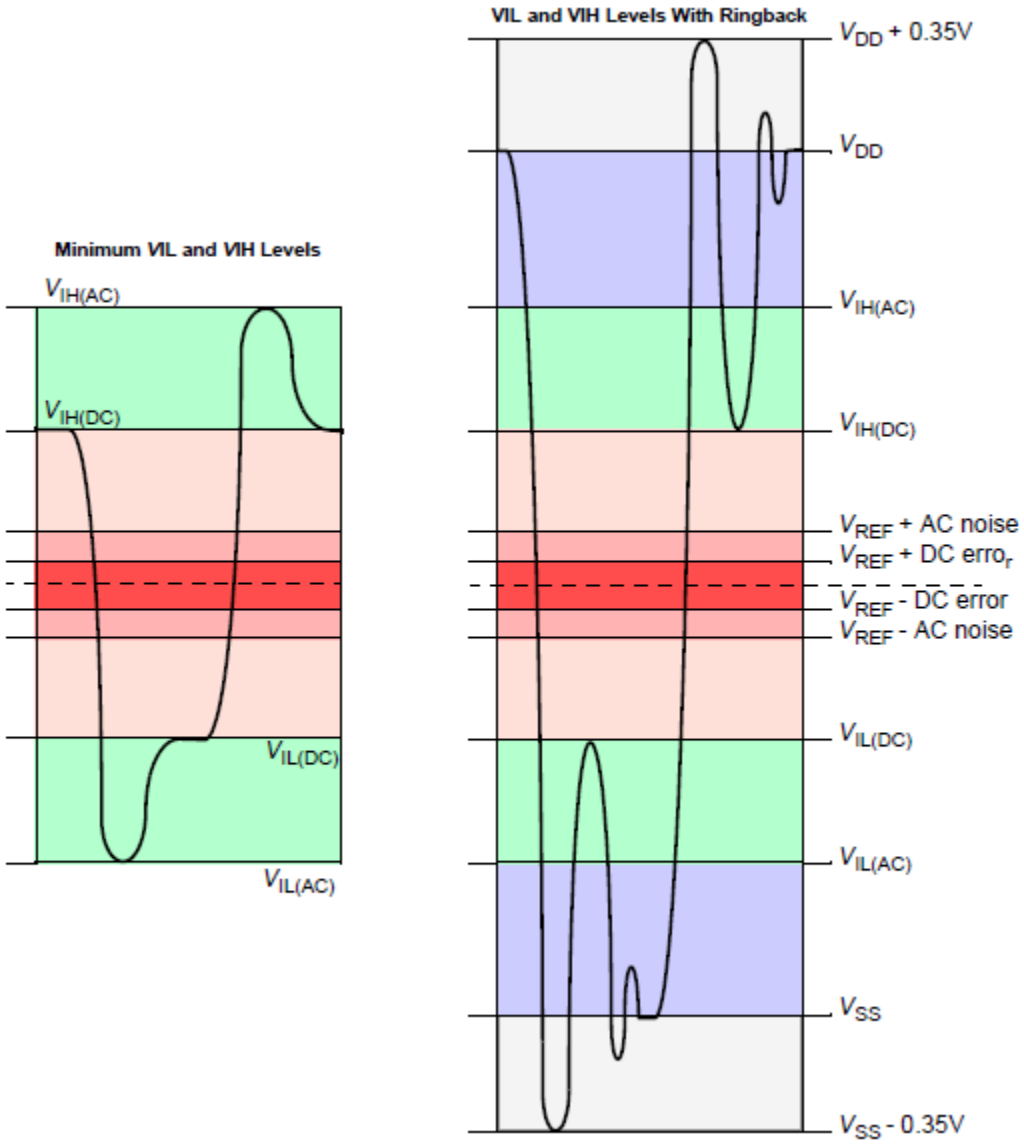


Figure. LPDDR3 Input signal

Note:
1. Numbers reflect nominal values.
2. For CA0-9, CK_t, CK_c and CS_n, VDD stands for VDDCA. For DQ, DM/DNV, DQS_t and DQS_c, VDD stands for VDDQ.
3. For CA0-9, CK_t, CK_c and CS_n, VSS stands for VSSCA. For DQ, DM/DNV, DQS_t and DQS_c, VSS stands for VSSQ.

AC and DC Logic Input Levels for Differential Signals

Differential Signal Definition

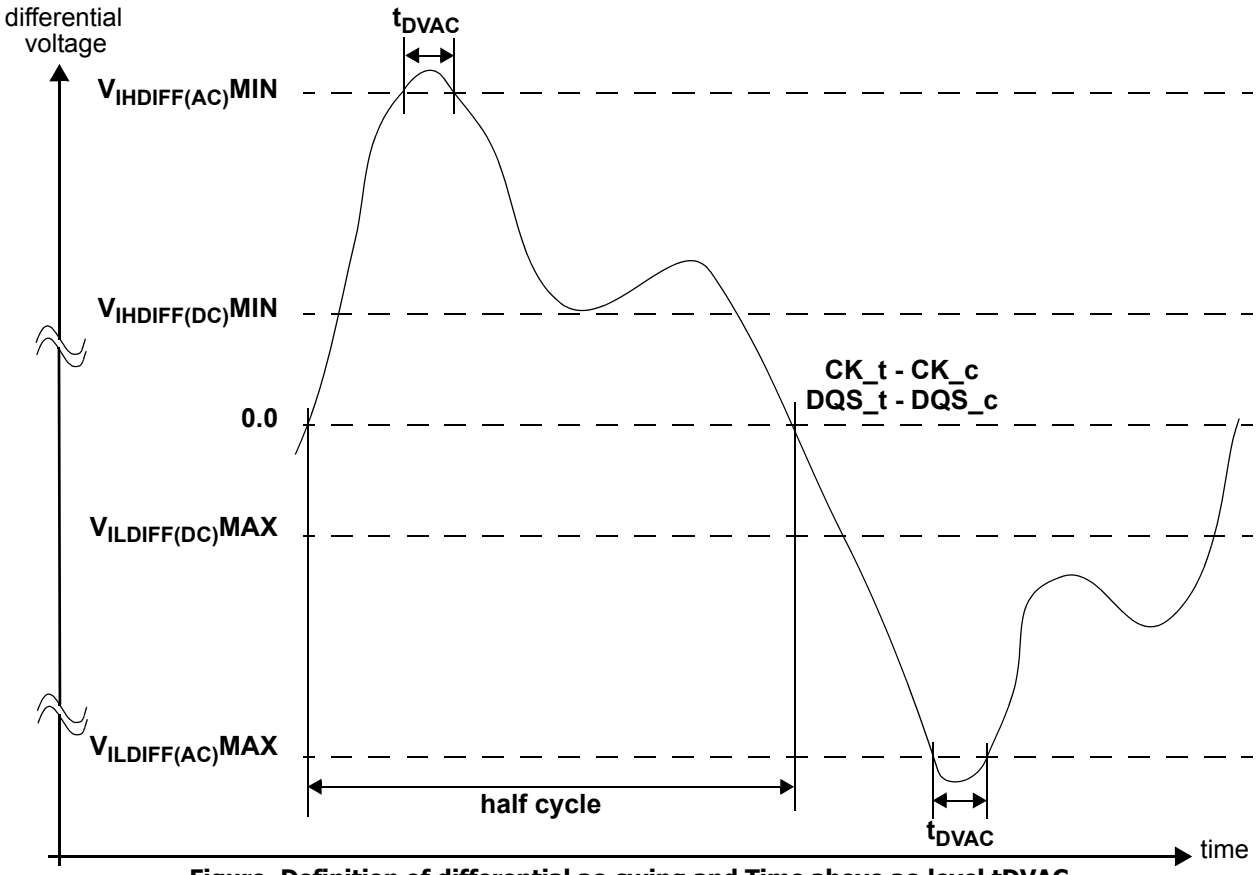


Figure. Definition of differential ac-swing and Time above ac-level tDVAC

Differential swing requirements for clock and strobe

Parameter	Symbol	Min	Max	Unit	Note
DC Differential Input High	VIHDIFF(DC)	2 x (VIH(DC) - VREF)	Note 3	V	1
DC Differential Input Low	VILDIFF(DC)	Note 3	2 x (VIL(DC) - VREF)	V	1
AC Differential Input High	VIHDIFF(AC)	2 x (VIH(AC) - VREF)	Note 3	V	2
AC Differential Input Low	VILDIFF(AC)	Note 3	2 x (VIL(AC) - VREF)	V	2

Note:
1. Used to define a differential signal slew-rate. For CK_t - CK_c use VIH/VIL(dc) of CA and VREFCA; for DQS_t - DQS_c, use VIH/VIL(dc) of DQs and VREFDQ; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.
2. For CK_t - CK_c use VIH/VIL(ac) of CA and VREFCA; for DQS_t - DQS_c, use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK_t, CK_c, DQS_t, and DQS_c need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to the section of "Overshoot and Undershoot Specifications".
4. For CK_t and CK_c, Vref = VrefCA(DC). For DQS_t and DQS_c, Vref = VrefDQ(DC).

Table. Allowed time before ringback (tDVAC) for DQS_t - DQS_c

Slew Rate [V/ns]	t_{DVAC} [ps] @ |VIH/Ldiff(ac)| = 300mV	t_{DVAC} [ps] @ |VIH/Ldiff(ac)| = 300mV
	1600Mbps	1333Mbps
	MIN	MIN
> 8.0	48	58
8.0	48	58
7.0	46	56
6.0	43	53
5.0	40	50
4.0	35	45
3.0	27	37
<3.0	27	37

Table. Allowed time before ringback (tDVAC) for CK_t - CK_c

Slew Rate [V/ns]	t_{DVAC} [ps] @ |VIH/Ldiff(ac)| = 300mV	t_{DVAC} [ps] @ |VIH/Ldiff(ac)| = 300mV
	1600Mbps	1333Mbps
	MIN	MIN
> 8.0	48	58
8.0	48	58
7.0	46	56
6.0	43	53
5.0	40	50
4.0	35	45
3.0	27	37
<3.0	27	37

Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK_t, DQS_t, CK_c, or DQS_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c shall meet VSEH(AC)min / VSEL(AC)max in every half-cycle.

DQS_t, DQS_c shall meet VSEH(AC)min / VSEL(AC)max in every half-cycle proceeding and following a valid transition.

Note that the applicable ac-levels for CA and DQ's are different per speed-bin.

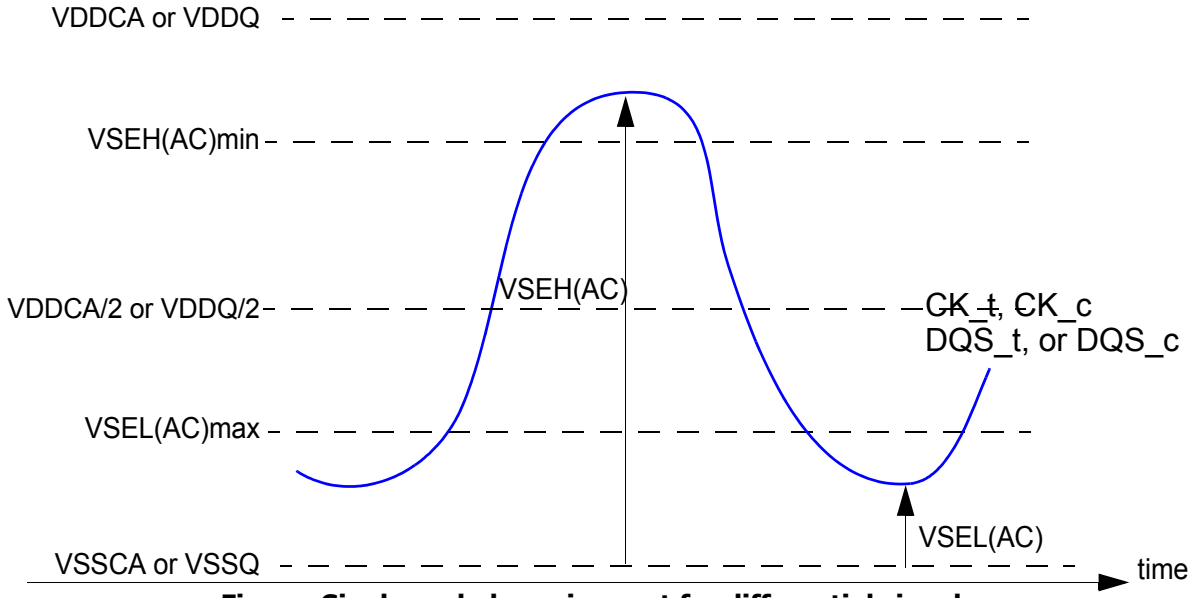


Figure. Single-ended requirement for differential signals

Note that while CA and DQ signal requirements are with respect to VREF, the single-ended components of differential signals have a requirement with respect to VDDQ/2 for DQS_t, DQS_C and VDDCA/2 for CK_t, CK_c; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL(AC)max, VSEH(AC)min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table. Single-ended Levels for Clock and Strobe

Parameter	Symbol	Min	Max	Unit	Note
Single-ended High Level for strobes	VSEH (AC150)	(VDDQ/2) + 0.150	Note 3	V	1, 2
Single-ended High Level for CK_t and CK_c		(VDDCA/2) + 0.150	Note 3	V	1, 2
Single-ended Low Level for strobes	VSEL (AC150)	Note 3	(VDDQ / 2) - 0.150	V	1, 2
Single-ended Low Level for CK_t and CK_c		Note 3	(VDDCA / 2) - 0.150	V	1, 2
Single-ended High Level for strobes	VSEH (AC135)	(VDDQ/2) + 0.135	Note 3	V	1, 2
Single-ended High Level for CK_t and CK_c		(VDDCA/2) + 0.135	Note 3	V	1, 2
Single-ended Low Level for strobes	VSEL (AC135)	Note 3	(VDDQ / 2) - 0.135	V	1, 2
Single-ended Low Level for CK_t and CK_c		Note 3	(VDDCA / 2) - 0.135	V	1, 2

Note:
1. For CK_t, CK_c use VSEH/VSEL(AC) of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use VIH/VIL(AC) of DQs.
2. VIH(AC)/VIL(AC) for DQs is based on VREFDQ; VSEH(AC)/VSEL(AC) for CA is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to the section of Overshoot and Undershoot Specifications.

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK_t, CK_c and DQS_t, DQS_c) must meet the requirements in "Single-ended Levels for Clock and Strobe". The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

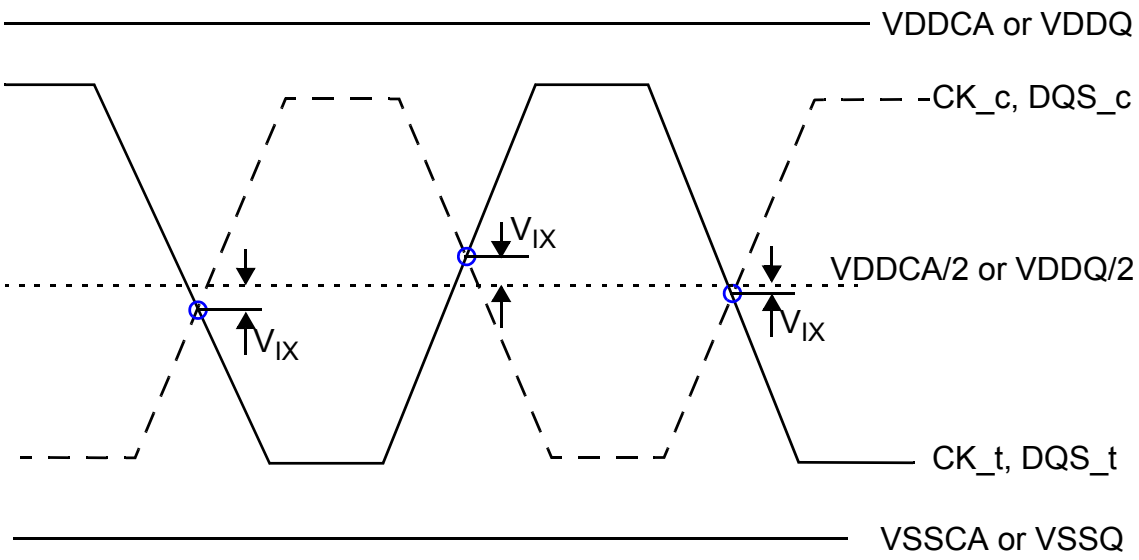


Figure. VIX definition

Table. Cross Point Voltage for Differential Input Signals (Clock and Strobe)

Parameter	Symbol	Min	Max	Unit	Note
Differential Input Cross Point Voltage relative to VDDCA/2 for CK_t and CK_c	VIXCA	-120	120	mV	1, 2
Differential Input Cross Point Voltage relative to VDDQ/2 for DQS_t and DQS_c	VIXDQ	-120	120	mV	1, 2

Note:

1. The typical value of VIX(AC) is expected to be about 0.5 x VDD of the transmitting device, and VIX(AC) is expected to track variations in VDD. VIX(AC) indicates the voltage at which differential input signals must cross.
2. For CK_t and CK_c, VREF = VREFCA(DC). For DQS_t and DQS_c, VREF = VREFDQ(DC).

Slew Rate Definitions for Single-ended Input Signals

See "CA and CS_n Setup, Hold and Derating" for single-ended slew rate definitions for address and command signals.
See "Data Setup, Hold and Slew Rate Derating" for single-ended slew rate definitions for data signals.

Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK_t, CK_c and DQS_t, DQS_c) are defined and measured as shown in below Table and Figure.

Table. Differential Input Slew Rate Definition

Parameter	Measured		Defined by
	From	To	
Differential Input Slew Rate for Rising Edge (CK_t - CK_c and DQS_t - DQS_c)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	[$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / Delta TRdiff
Differential Input Slew Rate for Falling Edge (CK_t - CK_c and DQS_t - DQS_c)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	[$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / Delta TFdiff

Note: 1. The differential signal (i.e. CK_t - CK_c and DQS_t - DQS_c) must be linear between these thresholds.

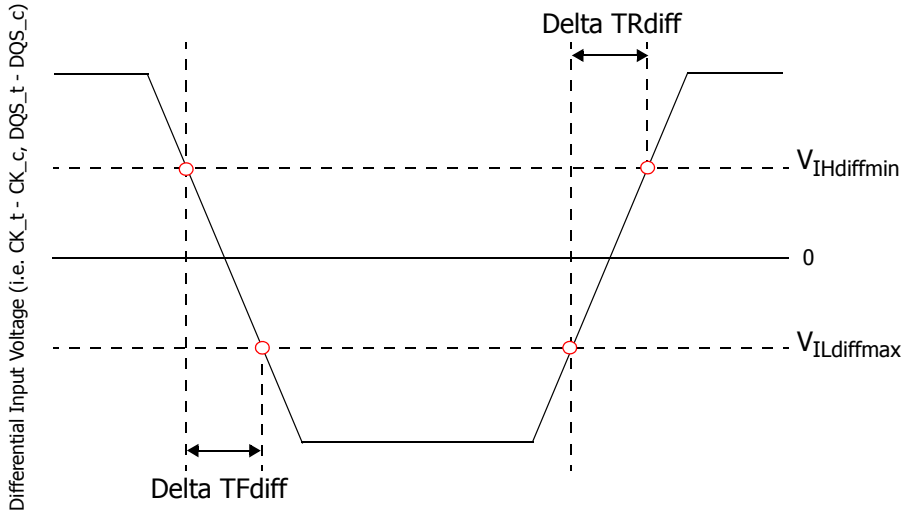


Figure. Differential Input Slew Rate Definition for CK_t, CK_c and DQS_t, DQS_c

AC and DC Output Measurement Levels

Single Ended AC and DC Output Levels

Parameter		Symbol	Levels	Unit	Note
DC Output Logic High Measurement Level (for IV curve linearity)		VOH(DC)	0.9 x VDDQ	V	1
DC Output Logic Low Measurement Level (for IV curve linearity)		VOL(DC)	0.1 x VDDQ	V	2
AC Output Logic High Measurement Level (for output slew rate)		VOH(AC)	VREFDQ + 0.12	V	
AC Output Logic Low Measurement Level (for output slew rate)		VOL(AC)	VREFDQ - 0.12	V	
Output Leakage current (DQ, DM, DQS_t and DQS_c) (DQ, DQS_t and DQS_c are disabled; 0V ≤ VOUT ≤ VDDQ)	Min	I_{OZ}	-5	uA	
	Max		5	uA	
Delta RON between pull-up and pull-down for DQ and DM	Min	MM_{PUPD}	-15	%	
	Max		15	%	

Note:
1. IOH = -0.1mA,
2. IOL = 0.1mA

Differential AC and DC Output Levels (DQS_t, DQS_c)

Parameter	Symbol	Levels	Unit	Note
AC Differential Output High measurement Level (for Output SR)	VOHdiff(AC)	+ 0.20 x VDDQ	V	
AC Differential Output Low measurement Level (for Output SR)	VOLdiff(AC)	- 0.20 x VDDQ	V	

Note:
1. IOH = -0.1mA,
2. IOL = 0.1mA

Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in below Table and Figure.

Parameter	Measured		Defined by
	From	To	
Single Ended Output Slew Rate for Rising Edge	VOL(AC)	VOH(AC)	[VOH(AC) - VOL(AC)] / Delta TRse
Single Ended Output Slew Rate for Falling Edge	VOH(AC)	VOL(AC)	[VOH(AC) - VOL(AC)] / Delta TFse

Note: Output slew rate is verified by design and characterization and may not be subject to production test.

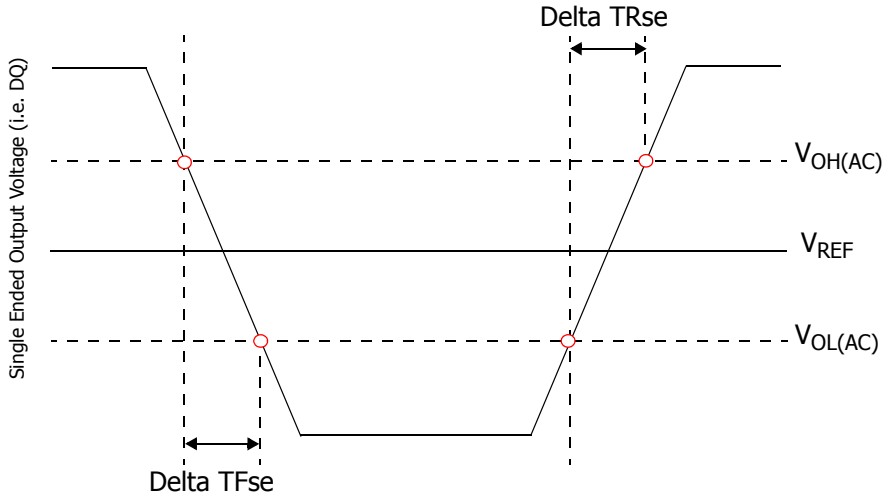


Figure. Single Ended Output Slew Rate Definition

Table. Output Slew Rate (Single Ended)

Parameter	Symbol	Min	Max	Unit	Note
Single-ended Output Slew Rate (RON = 40Ω +/- 30%)	SRQse	1.5	4.0	V/ns	
Output slew-rate matching Ratio (Pull-up to Pull-down)		0.7	1.4		

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

Note:

1. Measured with output reference load.
2. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
3. The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
4. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in below Table and Figure.

Parameter	Measured		Defined by
	From	To	
Differential Output Slew Rate for Rising Edge	$V_{OLdiff(AC)}$	$V_{OHdiff(AC)}$	[$V_{OHdiff(AC)}$ - $V_{OLdiff(AC)}$] / Delta TRdiff
Differential Output Slew Rate for Falling Edge	$V_{OHdiff(AC)}$	$V_{OLdiff(AC)}$	[$V_{OHdiff(AC)}$ - $V_{OLdiff(AC)}$] / Delta TFdiff

Note: 1. Output slew rate is verified by design and characterization, and may not be subject to production test.

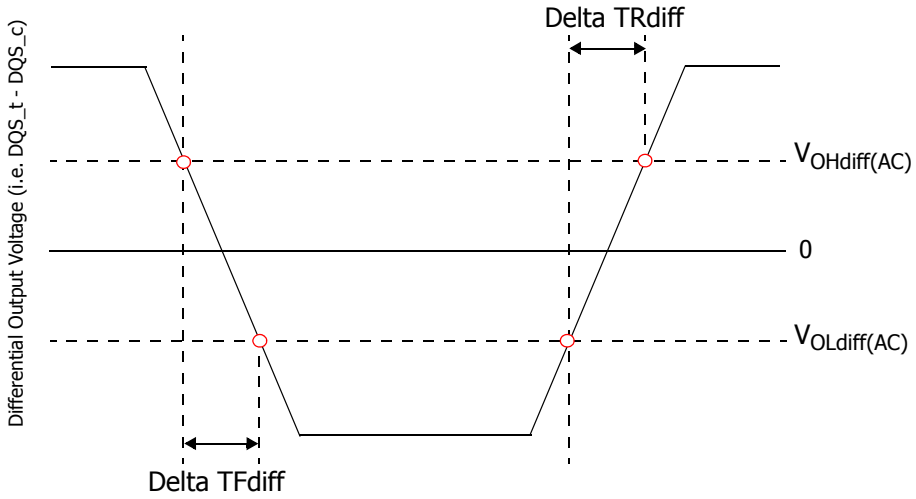


Figure. Differential Output Slew Rate Definition

Table. Output Slew Rate (Differential)

Parameter	Symbol	Min	Max	Unit	Note
Differential Output Slew Rate (RON = 40Ω +/- 30%)	SRQdiff	3.0	8.0	V/ns	

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: Differential Signals

Note:

1. Measured with output reference load.
2. The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
3. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

Overshoot and Undershoot Specifications

Parameter	1600	1333	Unit
Maximum peak amplitude allowed for overshoot area	0.35		V
Maximum peak amplitude allowed for undershoot area	0.35		V
Maximum overshoot area above VDD	0.10	0.12	V-ns
Maximum undershoot area below VSS	0.10	0.12	V-ns

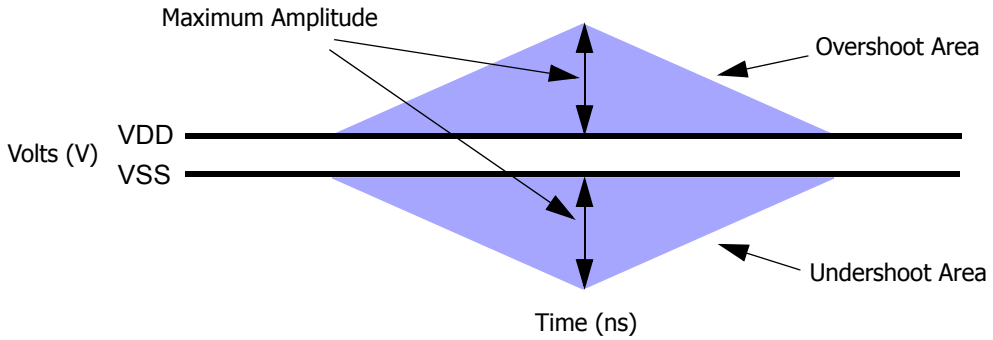


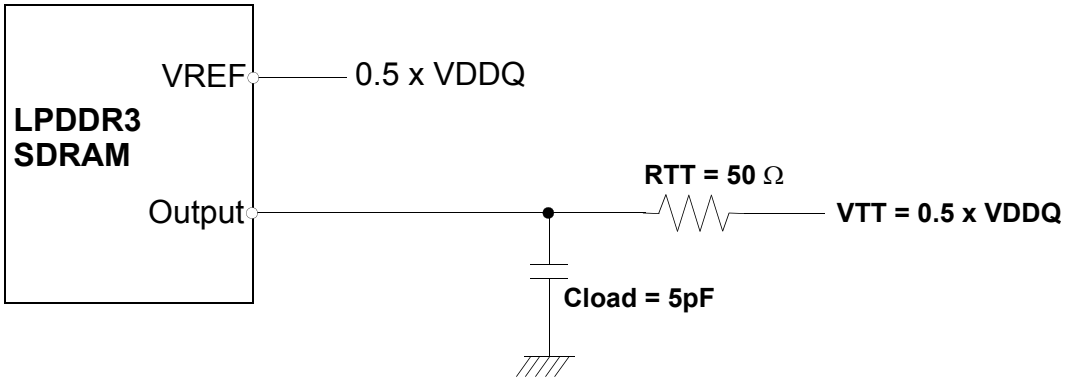
Figure. Overshoot and Undershoot Definition

Note:
1. VDD stands for VDDCA for CA0-9, CK_t, CK_c, CS_n, and CKE. VDD stands for VDDQ for DQ, DM, DQS_t, and DQS_c.
2. VSS stands for VSSCA for CA0-9, CK_t, CK_c, CS_n, and CKE. VSS stands for VSSQ for DQ, DM, DQS_t, and DQS_c.
3. Absolute maximum requirements apply.
4. Maximum peak amplitude values are referenced from actual VDD and VSS values.
5. Maximum area values are referenced from maximum operating VDD and VSS values.

Output Buffer Characteristics

HSUL_12 Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



Note: 1. All output timing parameter values (like t_{DQSCK}, t_{DQSQ}, t_{QHS}, t_{HZ}, t_{RPRE} etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

Figure. HSUL_12 Driver Output Reference Load for Timing and Slew Rate

RON_{PU} and RON_{PD} resistor Definition

$$RONPU = \frac{(VDDQ - Vout)}{ABS(Iout)}$$

Note 1: This is under the condition that RON_{PD} is turned off

$$RONPD = \frac{Vout}{ABS(Iout)}$$

Note 1: This is under the condition that RON_{PU} is turned off

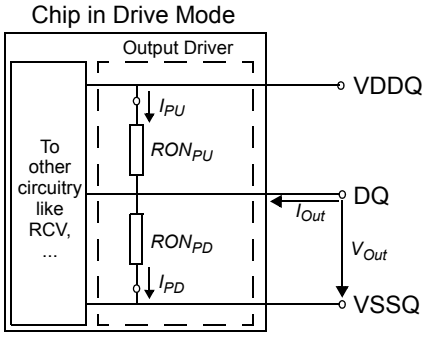


Figure. Output Driver: Definition of Voltages and Currents

RON_{PU} and RON_{PD} Characteristics with ZQ Calibration

Output driver impedance RON is defined by the value of the external reference resistor RZQ. Nominal RZQ is 240Ω.

Table - Output Driver DC Electrical Characteristics with ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Typ	Max	Unit	Notes
34.3Ω	RON34PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
	RON34PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
40.0Ω	RON40PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
	RON40PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
48.0Ω	RON48PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
	RON48PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
Mismatch between pull-up and pull-down	MM_{PUPD}		-15.00		+15.00	%	1,2,3,4,5

Note:
1. Across entire operating temperature range, after calibration.
2. RZQ = 240Ω.
3. The tolerance limits are specified after calibration with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
4. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x VDDQ.
5. Measurement definition for mismatch between pull-up and pull-down,
   MMPUPD: Measure RON_{PU} and RON_{PD}, both at 0.5 x VDDQ:

$$MMPUPD = \frac{RONPU - RONPD}{RONNOM} \times 100$$

For example, with MMPUPD(max) = 15% and RONPD = 0.85, RONPU must be less than 1.0.

Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

Table. Output Driver Sensitivity Definition

Resistor	Vout	Min	Max	Unit	Notes
RONPD	0.5 x VDDQ	85 - (*dRONdT* x |*ΔT*|) - (*dRONdV* x|*ΔV*|)	115 + (*dRONdT* x |*ΔT*|) + (*dRONdV* x|*ΔV*|)	%	1,2
RONPU					
RTT	0.5 x VDDQ	85 - (*dRTTdT* x |*ΔT*|) - (*dRTTdV* x|*ΔV*|)	115 + (*dRTTdT* x |*ΔT*|) + (*dRTTdV* x|*ΔV*|)	%	1,2

Note
1. *ΔT = T* - *T*(@ calibration), *ΔV = V* - *V*(@ calibration)
2. dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

Table. Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
dRONdT	RON Temperature Sensitivity	0.00	0.75	% / C
dRONdV	RON Voltage Sensitivity	0.00	0.20	% / mV
dRTTdT	RTT Temperature Sensitivity	0.00	0.75	% / C
dRTTdV	RTT Voltage Sensitivity	0.00	0.20	% / mV

RON_{PU} and RON_{PD} Characteristics without ZQ Calibration

Output driver impedance RON is defined by design and characterization as default setting.

Table. Output Driver DC Electrical Characteristics without ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3Ω	RON40PD	0.5 x VDDQ	24	34.3	44.6	Ω	1
	RON40PU	0.5 x VDDQ	24	34.3	44.6	Ω	1
40.0Ω	RON40PD	0.5 x VDDQ	28	40	52	Ω	1
	RON40PU	0.5 x VDDQ	28	40	52	Ω	1
48.0Ω	RON48PD	0.5 x VDDQ	33.6	48	62.4	Ω	1
	RON48PU	0.5 x VDDQ	33.6	48	62.4	Ω	1
60.0Ω (optional)	RON60PD	0.5 x VDDQ	42	60	78	Ω	1
	RON60PU	0.5 x VDDQ	42	60	78	Ω	1
80.0Ω (optional)	RON80PD	0.5 x VDDQ	56	80	104	Ω	1
	RON80PU	0.5 x VDDQ	56	80	104	Ω	1

Note:
1. Across entire operating temperature range, without calibration.

RZQ I-V Curve

Table. RZQ I-V Curve

Voltage(V)	RON = 240Ω (RZQ)							
	Pull-Down				Pull-Up			
	Current [mA] / RON [Ω]				Current [mA] / RON [Ω]			
	default value after ZQReset		with Calibration		default value after ZQReset		with Calibration	
	Min	Max	Min	Max	Min	Max	Min	Max
	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]
0.00	0.00	0.00	n/a	n/a	0.00	0.00	n/a	n/a
0.05	0.17	0.35	n/a	n/a	-0.17	-0.35	n/a	n/a
0.10	0.34	0.70	n/a	n/a	-0.34	-0.70	n/a	n/a
0.15	0.50	1.03	n/a	n/a	-0.50	-1.03	n/a	n/a
0.20	0.67	1.39	n/a	n/a	-0.67	-1.39	n/a	n/a
0.25	0.83	1.73	n/a	n/a	-0.83	-1.73	n/a	n/a
0.30	0.97	2.05	n/a	n/a	-0.97	-2.05	n/a	n/a
0.35	1.13	2.39	n/a	n/a	-1.13	-2.39	n/a	n/a
0.40	1.26	2.71	n/a	n/a	-1.26	-2.71	n/a	n/a
0.45	1.39	3.01	n/a	n/a	-1.39	-3.01	n/a	n/a
0.50	1.51	3.32	n/a	n/a	-1.51	-3.32	n/a	n/a
0.55	1.63	3.63	n/a	n/a	-1.63	-3.63	n/a	n/a
0.60	1.73	3.93	2.17	2.94	-1.73	-3.93	-2.17	-2.94
0.65	1.82	4.21	n/a	n/a	-1.82	-4.21	n/a	n/a
0.70	1.90	4.49	n/a	n/a	-1.90	-4.49	n/a	n/a
0.75	1.97	4.74	n/a	n/a	-1.97	-4.74	n/a	n/a
0.80	2.03	4.99	n/a	n/a	-2.03	-4.99	n/a	n/a
0.85	2.07	5.21	n/a	n/a	-2.07	-5.21	n/a	n/a
0.90	2.11	5.41	n/a	n/a	-2.11	-5.41	n/a	n/a
0.95	2.13	5.59	n/a	n/a	-2.13	-5.59	n/a	n/a
1.00	2.17	5.72	n/a	n/a	-2.17	-5.72	n/a	n/a
1.05	2.19	5.84	n/a	n/a	-2.19	-5.84	n/a	n/a
1.10	2.21	5.95	n/a	n/a	-2.21	-5.95	n/a	n/a
1.15	2.23	6.03	n/a	n/a	-2.23	-6.03	n/a	n/a
1.20	2.25	6.11	n/a	n/a	-2.25	-6.11	n/a	n/a

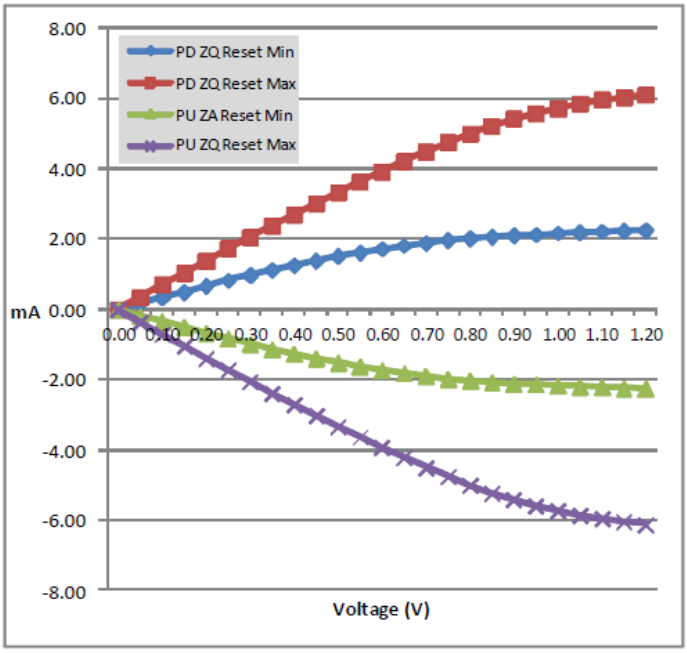


Figure. I-V Curve After ZQ Reset

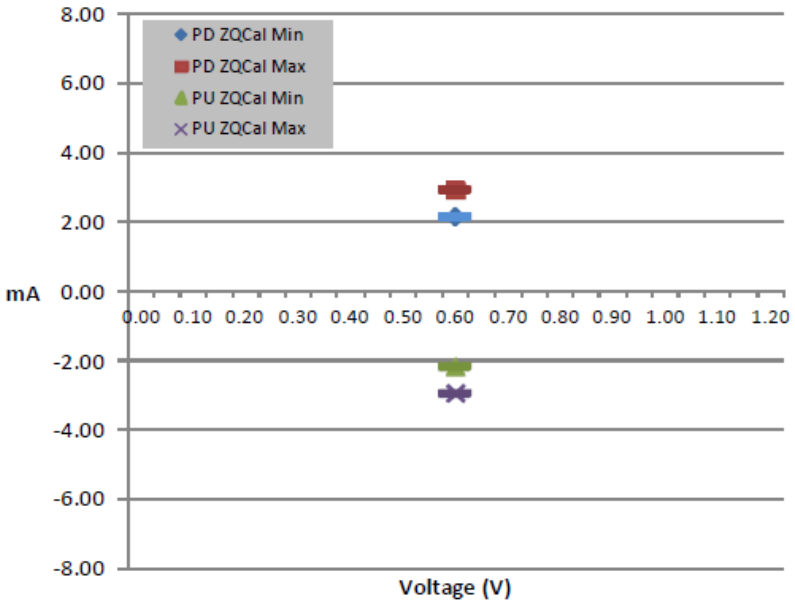


Figure. I-V Curve After Calibration

Input/Output Capacitance

Parameter	Symbol	Min	Max	Unit	Note
Input capacitance, CK_t and CK_c	CCK	0.50	1.2	pF	1,2
Input capacitance delta, CK_t and CK_c	CDCK	0	0.15	pF	1,2,3
Input capacitance, all other input-only pins	CI	0.50	1.1	pF	1,2,4
Input capacitance delta, all other input-only pins	CDI	-0.2	0.2	pF	1,2,5
Input/output capacitance, DQ, DM, DQS_t, DQS_c	CIO	1.0	1.8	pF	1,2,6,7
Input/output capacitance delta, DQS_t and DQS_c	CDDQS	0	0.2	pF	1,2,7,8
Input/output capacitance delta, DQ and DM	CDIO	-0.25	0.25	pF	1,2,7,9
Input/Output Capacitance ZQ	CZQ	0	2.0	pF	1,2

(TOPER; VDDQ = 1.14-1.3V; VDDCA = 1.14-1.3V; VDD1 = 1.7-1.95V, VDD2 = 1.14-1.3V)

Note:
1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSCA, VSSQ applied and all other pins floating).
3. Absolute value of CCK_t - CCK_c.
4. CI applies to CS_n, CKE, CA0-CA9.
5. CDI = CI - 0.5 * (CCK_t + CCK_c)
6. DM loading matches DQ and DQS.
7. MR3 I/O configuration DS OP3-OP0 = 0001B (34.3 Ohm typical)
8. Absolute value of CDQS_t and CDQS_c.
9. CDIO = CIO - 0.5 * (CDQS_t + CDQS_c) in byte-lane.

IDD Specification Parameters and Test Conditions

IDD Measurement Conditions

The following definitions are used within the IDD measurement tables:

LOW: $V_{IN} \leq V_{IL}$(DC) MAX

HIGH: VIN $\geq V_{IH}$(DC) MIN

STABLE: Inputs are stable at a HIGH or LOW level.

SWITCHING: See tables below.

Table. Switching for CA Input Signals

Switching for CA								
	CK_t (Rising) / CK_c (Falling)	CK_t (Falling) / CK_c (Rising)	CK_t (Rising) / CK_c (Falling)	CK_t (Falling) / CK_c (Rising)	CK_t (Rising) / CK_c (Falling)	CK_t (Falling) / CK_c (Rising)	CK_t (Rising) / CK_c (Falling)	CK_t (Falling) / CK_c (Rising)
Cycle	N		N+1		N+2		N+3	
CS_n	HIGH		HIGH		HIGH		HIGH	
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA6	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA7	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA8	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA9	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

Note:
1. CS_n must always be driven HIGH.
2. For each clock cycle, 50% of the CA bus is changing between HIGH and LOW once per clock for the CA bus.
3. The above pattern (N, N+1, N+2, N+3...) is used continuously during IDD measurement for IDD values that require switching on the CA bus.

Table. Switching for IDD4R

Clock	CKE	CS_n	Clock Cycle Number	Command	CA[0:2]	CA[3:9]	All DQs
Rising	HIGH	LOW	N	Read_Rising	HLH	LHLHLHL	L
Falling	HIGH	LOW	N	Read_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N+1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+1	NOP	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N+2	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+2	NOP	LLL	LLLLLLL	H
Rising	HIGH	HIGH	N+3	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+3	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N+4	Read_Rising	HLH	HLHLLHL	H
Falling	HIGH	LOW	N+4	Read_Falling	LHH	HHHHHHH	H
Rising	HIGH	HIGH	N+5	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N+5	NOP	HHH	HHHHHHH	L
Rising	HIGH	HIGH	N+6	NOP	HHH	HHHHHHH	L
Falling	HIGH	HIGH	N+6	NOP	HHH	HHHHHHH	L
Rising	HIGH	HIGH	N+7	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N+7	NOP	HLH	LHLHLHL	L

Note:
1. Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2. The above pattern (N, N+1, ...) is used continuously during IDD measurement for IDD4R.

Table. Switching for IDD4W

Clock	CKE	CS_n	Clock Cycle Number	Command	CA[0:2]	CA[3:9]	All DQs
Rising	HIGH	LOW	N	Write_Rising	HLL	LHLHLHL	L
Falling	HIGH	LOW	N	Write_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N+1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+1	NOP	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N+2	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+2	NOP	LLL	LLLLLLL	H
Rising	HIGH	HIGH	N+3	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+3	NOP	HLL	HLHLLHL	L
Rising	HIGH	LOW	N+4	Write_Rising	HLL	HLHLLHL	H
Falling	HIGH	LOW	N+4	Write_Falling	LHH	HHHHHHH	H
Rising	HIGH	HIGH	N+5	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N+5	NOP	HHH	HHHHHHH	L
Rising	HIGH	HIGH	N+6	NOP	HHH	HHHHHHH	L
Falling	HIGH	HIGH	N+6	NOP	HHH	HHHHHHH	L
Rising	HIGH	HIGH	N+7	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N+7	NOP	HLL	LHLHLHL	L

Note:
1. Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2. Data masking (DM) must always be driven LOW.
3. The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4W.

IDD specifications (1/2)

- All IDD values are single-die-equivalent values. Total current consumption is dependent to user operating condition.

Parameter / Test Condition	Symbol	Power Supply	1600	Unit	Note
Operating one bank active-precharge current: tCK = tCKmin; tRC = tRCmin; CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD0_1$	VDD1	10	mA	
	$IDD0_2$	VDD2	30	mA	
	$IDD0_{IN}$	VDDCA VDDQ	7	mA	4
Idle power-down standby current: tCK = tCKmin; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD2P_1$	VDD1	0.5	mA	
	$IDD2P_2$	VDD2	2	mA	
	$IDD2P_{IN}$	VDDCA VDDQ	0.2	mA	4,8
Idle power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD2PS_1$	VDD1	0.5	mA	
	$IDD2PS_2$	VDD2	2	mA	
	$IDD2PS_{IN}$	VDDCA VDDQ	0.2	mA	4,8
Idle non-power-down standby current: tCK = tCKmin; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD2N_1$	VDD1	2	mA	
	$IDD2N_2$	VDD2	5	mA	
	$IDD2N_{IN}$	VDDCA VDDQ	7	mA	4
Idle non-power-down standby current with clock stopped: CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD2NS_1$	VDD1	2	mA	
	$IDD2NS_2$	VDD2	3	mA	
	$IDD2NS_{IN}$	VDDCA VDDQ	7	mA	4
Active power-down standby current: tCK = tCKmin; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD3P_1$	VDD1	2	mA	
	$IDD3P_2$	VDD2	6	mA	
	$IDD3P_{IN}$	VDDCA VDDQ	0.2	mA	4,8
Active power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD3PS_1$	VDD1	2	mA	
	$IDD3PS_2$	VDD2	6	mA	
	$IDD3PS_{IN}$	VDDCA VDDQ	0.2	mA	4,8
Active non-power-down standby current: tCK = tCKmin; CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD3N_1$	VDD1	2	mA	
	$IDD3N_2$	VDD2	8	mA	
	$IDD3N_{IN}$	VDDCA VDDQ	7	mA	4

IDD specifications (2/2)

- All IDD values are single-die-equivalent values. Total current consumption is dependent to user operating condition.

Parameter / Test Condition	Symbol	Power Supply	1600	Unit	Note
Active non-power-down standby current with clock stopped: CK = LOW, CK# = HIGH CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD3NS_1$	VDD1	2	mA	
	$IDD3NS_2$	VDD2	6	mA	
	$IDD3NS_{IN}$	VDDCA VDDQ	7	mA	4
Operating burst READ current: tCK = tCKmin; CS_n is HIGH between valid commands; One bank is active; BL = 8; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer ODT disabled	$IDD4R_1$	VDD1	8	mA	
	$IDD4R_2$	VDD2	220	mA	
	$IDD4R_{IN}$	VDDCA	8	mA	
	$IDD4R_Q$	VDDQ	230	mA	5
Operating burst WRITE current: tCK = tCKmin; CS_n is HIGH between valid commands; One bank is active; BL = 8; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	$IDD4W_1$	VDD1	8	mA	
	$IDD4W_2$	VDD2	210	mA	
	$IDD4W_{IN}$	VDDCA VDDQ	25	mA	4

All-bank REFRESH burst current:
tCK = tCKmin; CKE is HIGH between valid commands;
tRC = tRFCabmin;
Burst refresh;
CA bus inputs are switching; Data bus inputs are stable
ODT disabled
	$IDD5_1$	VDD1	50	mA	

	$IDD5_2$	VDD2	120	mA	
	$IDD5_{IN}$	VDDCA VDDQ	7	mA	4

All-bank REFRESH average current:
tCK = tCKmin; CKE is HIGH between valid commands;
tRC = tREFI;
CA bus inputs are switching; Data bus inputs are stable
ODT disabled
	$IDD5ab_1$	VDD1	4	mA	

	$IDD5ab_2$	VDD2	10	mA	
	$IDD5ab_{IN}$	VDDCA VDDQ	7	mA	4

Per-bank REFRESH average current:
tCK = tCKmin; CKE is HIGH between valid commands;
tRC = tREFI/8;
CA bus inputs are switching; Data bus inputs are stable
ODT disabled
	$IDD5pb_1$	VDD1	4	mA	

	$IDD5pb_2$	VDD2	10	mA	
	$IDD5pb_{IN}$	VDDCA VDDQ	7	mA	4
Self refresh current (–30°C to +85°C): CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable Maximum 1x self refresh rate ODT disabled	$IDD6_1$	VDD1	2	mA	6
	$IDD6_2$	VDD2	4.5	mA	6
	$IDD6_{IN}$	VDDCA VDDQ	0.2	mA	4,6,8
Self refresh current (+85°C to +105°C): CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD6ET_1$	VDD1	5	mA	6,7
	$IDD6ET_2$	VDD2	12	mA	6,7
	$IDD6ET_{IN}$	VDDCA VDDQ	0.4	mA	4,6,7,8

Note:

1. Published IDD values are the maximum of the distribution of the arithmetic mean at 85°C.
2. IDD current specifications are tested after the device is properly initialized.
3. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh, before going into the elevated temperature range.
4. Measured currents are the summation of VDDQ and VDDCA.
5. Guaranteed by design with output load = 5 pF and RON = 40 ohm.
6. This is the general definition that applies to full-array SELF REFRESH.
7. IDD6ET is a typical value, is sampled only, and is not tested.
8. For all IDD measurements, VIHCKE = 0.8 x VDDCA, VILCKE = 0.2 x VDDCA.

IDD6 Partial Array Self Refresh Current

Temp. (°C)	Memory Array				Unit
	8 Banks	4 Banks	2 Banks	1 Bank	
-25	0.40 / 0.75 / 0.05	0.70 / 0.61 / 0.05	0.35 / 0.54 / 0.05	0.35 / 0.50 / 0.05	mA
25	0.41 / 0.80 / 0.05	0.38 / 0.80 / 0.05	0.37 / 0.58 / 0.05	0.36 / 0.54 / 0.05	mA
45	0.82 / 1.60 / 0.05	0.76 / 1.32 / 0.05	0.74 / 1.18 / 0.05	0.72 / 1.11 / 0.05	mA
85	2.00 / 4.50 / 0.20	1.60 / 3.18 / 0.20	1.38 / 2.52 / 0.20	1.26 / 2.18 / 0.20	mA
105	5.00 / 12.00 / 0.40	3.00 / 6.44 / 0.40	1.70 / 3.66 / 0.40	1.10 / 2.27 / 0.40	mA

Note:

1. IDD6 105°C is the typical , and the others are maximum value.
2. IDD6 currents are measured using bank-masking only.
3. IDD values published are the maximum of the distribution of the arithmetic mean.

AC TIMING PARAMETERS (1/5)

Parameter	Symbol	min max	LPDDR3 1600	LPDDR3 1066	LPDDR3 100	LPDDR3 50	Unit	Note
Maximum clock Frequency		-	800	533	50	25	MHz	
Clock Timing								
Average Clock Period	tCK(avg)	min	1.25	1.88	20.00	40.00	ns	
		max	100					
Average high pulse width	tCH(avg)	min	0.45				tCK(avg)	
		max	0.55					
Average low pulse width	tCL(avg)	min	0.45				tCK(avg)	
		max	0.55					
Absolute Clock Period	tCK(abs)	min	tCK(avg)min + tJIT(per)min				ns	
Absolute clock HIGH pulse width (with allowed jitter)	tCH(abs), allowed	min	0.43				tCK(avg)	
		max	0.57					
Absolute clock LOW pulse width (with allowed jitter)	tCL(abs), allowed	min	0.43				tCK(avg)	
		max	0.57					
Clock Period Jitter (with allowed jitter)	tJIT(per), allowed	min	-70	-90	-450	-850	ps	
		max	70	90	450	850		
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	tJIT(cc), allowed	max	140	180	900	1700	ps	
Duty cycle Jitter (with allowed jitter)	tJIT(duty), allowed	min	min((tCH(abs)min -tCH(avg)min), (tCL(abs)min - tCL(avg)min)) * tCK(avg)				ps	
		max	max((tCH(abs)max - tCH(avg)max), (tCH(abs)max - tCL(avg)max)) * tCK(avg)					
Cumulative error across 2 cycles	tERR(2per), allowed	min	-103	-132	-662	-1251	ps	
		max	103	132	662	1251		
Cumulative error across 3 cycles	tERR(3per), allowed	min	-122	-157	-786	-1485	ps	
		max	122	157	786	1485		
Cumulative error across 4 cycles	tERR(4per), allowed	min	-136	-175	-874	-1651	ps	
		max	136	175	874	1651		
Cumulative error across 5 cycles	tERR(5per), allowed	min	-147	-188	-942	-1780	ps	
		max	147	188	942	1780		
Cumulative error across 6 cycles	tERR(6per), allowed	min	-155	-200	-998	-1886	ps	
		max	155	200	998	1886		
Cumulative error across 7 cycles	tERR(7per), allowed	min	-163	-209	-1045	-1975	ps	
		max	163	209	1045	1975		
Cumulative error across 8 cycles	tERR(8per), allowed	min	-169	-217	-1086	-2052	ps	
		max	169	217	1086	2052		
Cumulative error across 9 cycles	tERR(9per), allowed	min	-175	-224	-1122	-2120	ps	
		max	175	224	1122	2120		
Cumulative error across 10 cycles	tERR(10per), allowed	min	-180	-231	-1155	-2181	ps	
		max	180	231	1155	2181		

AC TIMING PARAMETERS (2/5)

Parameter	Symbol	min max	LPDDR3 1600	LPDDR3 1066	LPDDR3 100	LPDDR3 50	Unit	Note
Clock Timing (continued)								
Cumulative error across 11 cycles	tERR(11per), allowed	min	-184	-237	-1184	-2236	ps	
		max	184	237	1184	2236		
Cumulative error across 12 cycles	tERR(12per), allowed	min	-188	-242	-1210	-2286	ps	
		max	188	242	1210	2286		
Cumulative error across n cycles (n = 13, 14 ,. . . ,20)	tERR(nper), allowed	min	tERR(nper),allowed min = (1 + 0.68ln(n)) * tJIT(per),allowed min				ps	
		max	tERR(nper),allowed max = (1 + 0.68ln(n)) * tJIT(per),allowed max					
ZQ Calibration Parameters								
Initialization Calibration Time	tZQINIT	min	1				us	
Long Calibration Time	tZQCL	min	360				ns	
Short Calibration Time	tZQCS	min	90				ns	
Calibration Reset Time	tZQRESET	min	max(50ns, 3nCK)				ns	
Read Parameters								3
DQS output access time from CK/CK#	tDQSCK	min	2.5				ns	
		max	5					
DQSCK Delta short	tDQSCKDS	max	220	330	3600	7200	ps	4
DQSCK Delta Medium	tDQSCKDM	max	511	680	2100	2100	ps	5
DQSCK Delta Long	tDQSCKDL	max	614	920	2400	2400	ps	6
DQS-DQ skew	tDQSQ	max	135	200	1300	2400	ps	
DQS Output High Pulse Width	tQSH	min	tCH(abs) - 0.05				tCK(avg)	
DQS Output Low Pulse Width	tQSL	min	tCL(abs) - 0.05				tCK(avg)	
DQ/DQS output hold time from DQS	tQH	min	MIN (tQSH, tQSL)				ps	
Read preamble	tRPRE	min	0.9				tCK(avg)	7,10
Read postamble	tRPST	min	0.3				tCK(avg)	7,11
DQS low-Z from clock	tLZ(DQS)	min	tDQSCK(min) - 300				ps	7
DQ low-Z from clock	tLZ(DQ)	min	tDQSCK(min) - 300				ps	7
DQS high-Z from clock	tHZ(DQS)	max	tDQSCK(max) - 100				ps	7
DQ high-Z from clock	tHZ(DQ)	max	tDQSCK(max) + (1.4 x tDQSQmax)				ps	7

AC TIMING PARAMETERS (3/5)

Parameter	Symbol	min max	LPDDR3 1600	LPDDR3 1066	LPDDR3 100	LPDDR3 50	Unit	Note
Write Parameters								3
DQ and DM input setup time (Vref based)	tDS	min	150	210	300	300	ps	
DQ and DM input hold time (Vref based)	tDH	min	150	210	300	300	ps	
DQ and DM input pulse width	tDIPW	min	0.35				tCK(avg)	
Write command to 1st DQS latching transition	tDQSS	min	0.75				tCK(avg)	
		max	1.25					
DQS input high-level width	tDQSH	min	0.4				tCK(avg)	
DQS input low-level width	tDQSL	min	0.4				tCK(avg)	
DQS falling edge to CK setup time	tDSS	min	0.2				tCK(avg)	
DQS falling edge hold time from CK	tDSH	min	0.2				tCK(avg)	
Write postamble	tWPST	min	0.4				tCK(avg)	
Write preamble	tWPRE	min	0.35				tCK(avg)	
CKE Input Parameters								
CKE min. pulse width (high/low pulse width)	tCKE	min	max(7.5ns, 3nCK)				ns	
CKE input setup time	tISCKE	min	0.25				tCK(avg)	12
CKE input hold time	tIHCKE	min	0.25				tCK(avg)	13
Command path disable delay	tCPDED	min	2				tCK(avg)	
Command Address Input Parameters								3
Address and control input setup time	tISCA	min	150	220	300	300	ps	14
Address and control input hold time	tIHCA	min	150	220	300	300	ps	14
CS_n input setup time	tISCS	min	270	300	300	300	ps	14
CS_n input hold time	tIHCS	min	270	300	300	300	ps	14
Address and control input pulse width	tIPWCA	min	0.35				tCK(avg)	
CS_n input pulse width	tIPWCS	min	0.7				tCK(avg)	
Boot Parameters (10MHz-55MHz)								15,16, 17
Clock Cycle Time	tCKb	min	18				ns	
		max	100					
CKE Input Setup Time	tISCKEb	min	300				ps	
CKE Input Hold Time	tIHCKEb	min	300				ps	
Address & Control Input Setup Time	tISb	min	300				ps	
Address & Control Input Hold Time	tIHb	min	300				ps	
DQS Output Data Access Time from CK/CK#	tDQSCKb	min	2.0				ns	
		max	10.0					
Data Strobe Edge to Output Data Edge tDQSQb	tDQSQb	max	1.2				ns	
Mode Register Parameters								
MODE REGISTER Write command period	tMRW	min	10	5	5	5	tCK(avg)	
MODE REGISTER Read command period	tMRR	min	4				tCK(avg)	
Additional time after tXP has expired until MRR command may be issued	tMRRI	min	tRCD(MIN)				ns	

AC TIMING PARAMETERS (4/5)

Parameter	Symbol	min max	LPDDR3 1600	LPDDR3 1066	LPDDR3 100	LPDDR3 50	Unit	Note
Core Parameters								18
Read Latency	RL	min	12	8	3	3	tCK(avg)	
Write Latency	WL	min	6	4	1	1	tCK(avg)	
ACTIVE to ACTIVE command period	tRC	min	tRAS+tRPab (with all-bank Precharge) tRAS+tRPpb (with per-bank Precharge)				ns	
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	tCKESR	min	max(15ns, 3nCK)				ns	
Self refresh exit to next valid command delay	tXSR	min	max(tRFCab +10ns, 2nCK)				ns	
Exit power down to next valid command delay	tXP	min	max(7.5ns, 3nCK)				ns	
CAS to CAS delay	tCCD	min	4				tCK(avg)	
Internal Read to Precharge command delay	tRTP	min	max(7.5ns, 4nCK)				ns	
RAS to CAS Delay	tRCD	min	max(18ns, 3nCK)				ns	
Row Precharge Time (single bank)	tRPpb	min	max(18ns ,3nCK)				ns	
Row Precharge Time (all banks) - 8-bank	tRPab	min	max(21ns, 3nCK)				ns	
Row Active Time	tRAS	min	max(42ns, 3nCK)				ns	
		max	70,000					
Write Recovery Time	tWR	min	max(15ns, 4nCK)				ns	
Internal Write to Read Command Delay	tWTR	min	max(7.5ns, 4nCK)				ns	
Active bank A to Active bank B	tRRD	min	max(10ns, 2nCK)				ns	
Four Bank Activate Window	tFAW	min	max(45ns, 8nCK)				ns	
Minimum Deep Power Down Time	tDPD	min	500				us	

AC TIMING PARAMETERS (5/5)

Parameter	Symbol	min max	LPDDR3 1600	LPDDR3 1066	LPDDR3 100	LPDDR3 50	Unit	Note
CA Training Parameters								
First CA calibratino command after CA calibration mode is programmed	tCAMRD	min	20				tCK(avg)	
First CA calibratino command after CKE is LOW	tCAENT	min	10				tCK(avg)	
CA calibration exit command after CKE is HIGH	tCAEXT	min	10				tCK(avg)	
CKE LOW after CA calibration mode is programmed	tCACKEL	min	10				tCK(avg)	
CKE HIGH after the last CA calibration results are driven	tCACKEH	min	10				tCK(avg)	
Data out delay after CA training calibration command is programmed	tADR	max	20				ns	
MRW CA exit command to DQ tri-state	tMRZ	min	3				ns	
CA calibration command to CA calibration command delay	tCACD	min	RU(tADR+2*tCK)				tCK(avg)	
Write Leveling Parameters								
DQS_t/DQS_c delay after write leveling mode is programmed	tWLDQSEN	min	25				ns	
		max	-					
First DQS_t/DQS_c edge after write leveling mode is programmed	tWLMRD	min	40				ns	
		max	-					
Write leveling output delay	tWLO	min	0				ns	
		max	20					
Write leveling hold time	tWLH	min	175	270	2800	5600	ps	
Write leveling setup time	tWLS	min	175	270	2800	5600	ps	
Mode register set command delay	tMRD	min	Max(14ns, 10nCK)				ns	
		max	-					
Temperature De-Rating								17
tDQSCK De-Rating	tDQSCK (Derated)	max	5620				ps	
Core Timings Temperature De-Rating	tRCD (Derated)	min	tRCD + 1.875				ns	
	tRC (Derated)	min	tRC + 1.875				ns	
	tRAS (Derated)	min	tRAS + 1.875				ns	
	tRP (Derated)	min	tRP + 1.875				ns	
	tRRD (Derated)	min	tRRD + 1.875				ns	

Note:
1. Frequency values are for reference only. Clock cycle time (tCK) is used to determine device capabilities.
2. All AC timings assume an input slew rate of 2 V/ns.
3. Measured with 4V/ns differential CK_t/CK_c slew rate and nominal VIX.
4. All timing and voltage measurements are defined 'at the ball'.
5. READ, WRITE, and input setup and hold values are referenced to VREF.
6. tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.
7. tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 1.6µs rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.
8. tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.
9. For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (VTT). tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Figure shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
10. Output Transition Timing

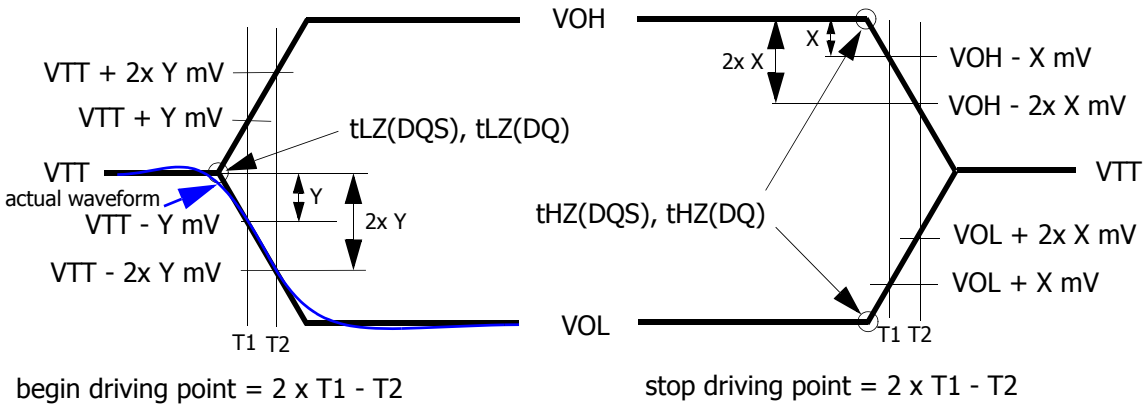


Figure. HSUL_12 Driver Output Reference Load for Timing and Slew Rate

11. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS/DQS#.
12. Measured from the point when DQS_t/DQS_c begins driving the signal to the point when DQS_t/DQS_c begins driving the first rising strobe edge.
13. Measured from the last falling strobe edge of DQS_t/DQS_c to the point when DQS_t/DQS_c finishes driving the signal.
14. CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK_t/CK_c crossing.
15. CKE input hold time is measured from CK_t/CK_c crossing to CKE reaching a HIGH/LOW voltage level.
16. Input set-up/hold time for signal (CA[9:0], CS_n).
17. To ensure device operation before the device is configured, a number of AC boot-timing parameters are defined in this table. Boot parameter symbols have the letter b appended (for example, tCK during boot is tCKb).
18. The LPDDR3 device will set some mode register default values upon receiving a RESET (MRW) command as specified in "Mode Register Definition".
19. The output skew parameters are measured with default output impedance settings using the reference load.
20. The minimum tCK column applies only when tCK is greater than 6ns.

CA and CS_n Setup, Hold and Derating

For all input signals (CA and CS_n) the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value to the ΔtIS and ΔtIH derating value respectively. Example: tIS (total setup time) = tIS(base) + ΔtIS

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC)max. If the actual signal is always earlier than the nominal slew rate line between shaded `VREF(DC) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded `VREF(DC) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VREF(DC). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VREF(DC). If the actual signal is always later than the nominal slew rate line between shaded `DC to VREF(DC) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded `DC to VREF(DC) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(DC) level is used for derating value.

For a valid transition the input signal has to remain above/below VIH/IL(AC) for some time tVAC.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(AC).

For slew rates in between the values listed in Table, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table. CA Setup and Hold Base-Values

unit [ps]	LPDDR3 1600	LPDDR3 1333	Reference
tIS(base)	75	100	VIH/L(AC)=VREF(DC)+/-150mV
tIH(base)	100	125	VIH/L(DC)=VREF(DC)+/-100mV

Note 1: AC/DC referenced for 2V/ns CA slew rate and 4V/ns differential CK_t/CK_c slew rate.

Table. CS_n Setup and Hold Base-Values

unit [ps]	LPDDR3 1600	LPDDR3 1333	Reference
tIS(base)	195	215	VIH/L(AC)=VREF(DC)+/-150mV
tIH(base)	220	240	VIH/L(DC)=VREF(DC)+/-100mV

Note 1: AC/DC referenced for 2V/ns CS_n slew rate and 4V/ns differential CK_t/CK_c slew rate.

Table. Derating values tIS/tIH - ac/dc based AC150

		ΔtISCA, ΔtIHCA, ΔtISCS, ΔtIHCS derating in [ps] AC/DC based AC150 Threshold -> VIH(ac)=VREF(dc)+150mV, VIL(ac)=VREF(dc)-150mV DC100 Threshold -> VIH(dc)=VREF(dc)+100mV, VIL(dc)=VREF(dc)-100mV											
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS_n Slew rate V/ns	4.0	38	25	38	25	38	25	38	25	38	25		
	3.0			25	17	25	17	25	17	25	17	38	29
	2.0					0	0	0	0	0	0	13	13
	1.5							-25	-17	-25	-17	-12	-4

Note 1: Cell contents shaded in red are defined as 'not supported'

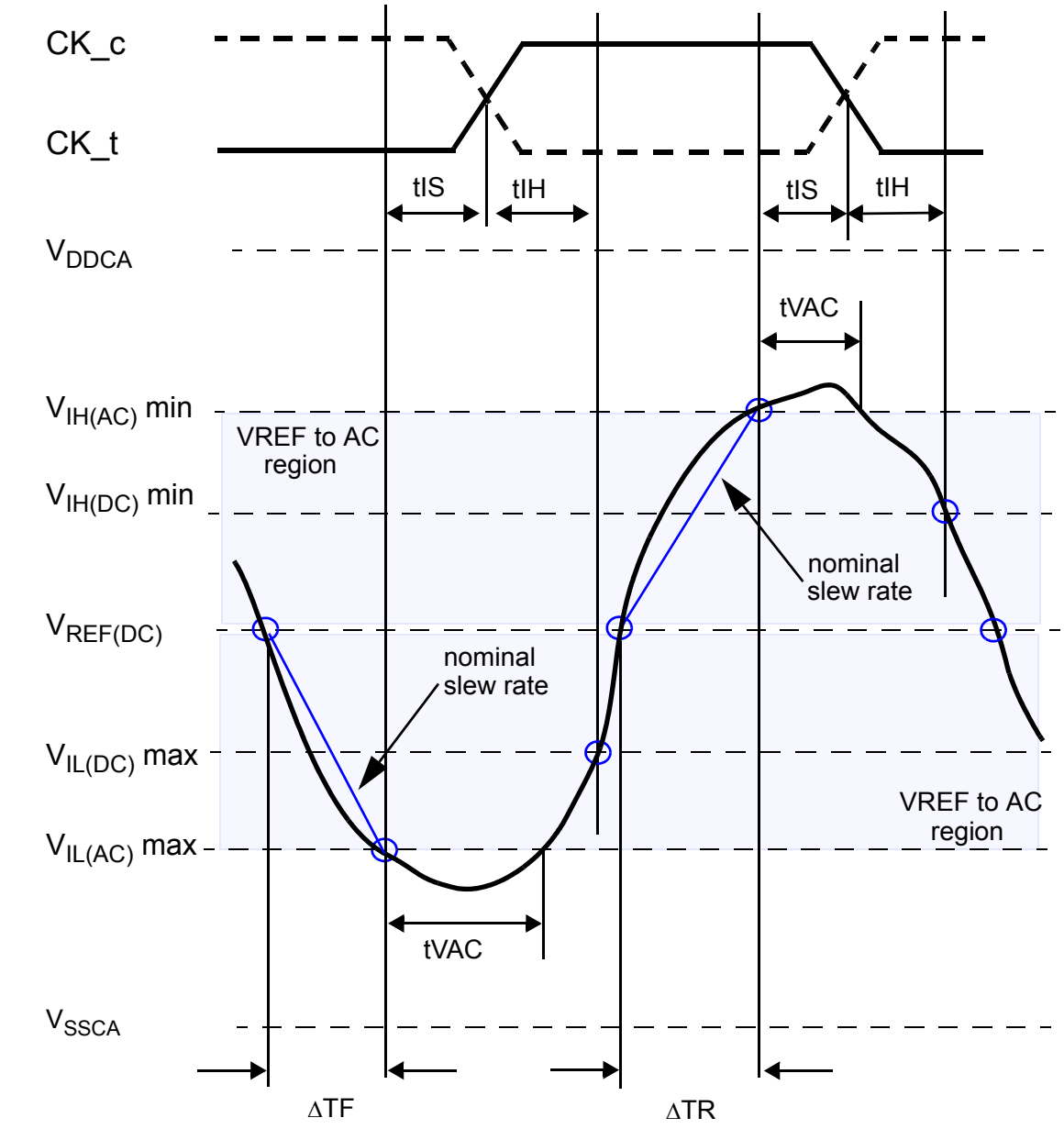
Table. Derating values tIS/tIH - ac/dc based AC135

		ΔtISCA, ΔtIHCA, ΔtISCS, ΔtIHCS derating in [ps] AC/DC based AC135 Threshold -> VIH(ac)=VREF(dc)+135mV, VIL(ac)=VREF(dc)-135mV DC100 Threshold -> VIH(dc)=VREF(dc)+100mV, VIL(dc)=VREF(dc)-100mV											
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS_n Slew rate V/ns	4.0	34	25	34	25	34	25	34	25	34	25		
	3.0			23	17	23	17	23	17	23	17	34	29
	2.0					0	0	0	0	0	0	11	13
	1.5							-23	-17	-23	-17	-12	-4

Note 1: Cell contents shaded in red are defined as 'not supported'

Table. Required time t_{VAC} above VIH(ac) {below VIL(ac)} for valid transition

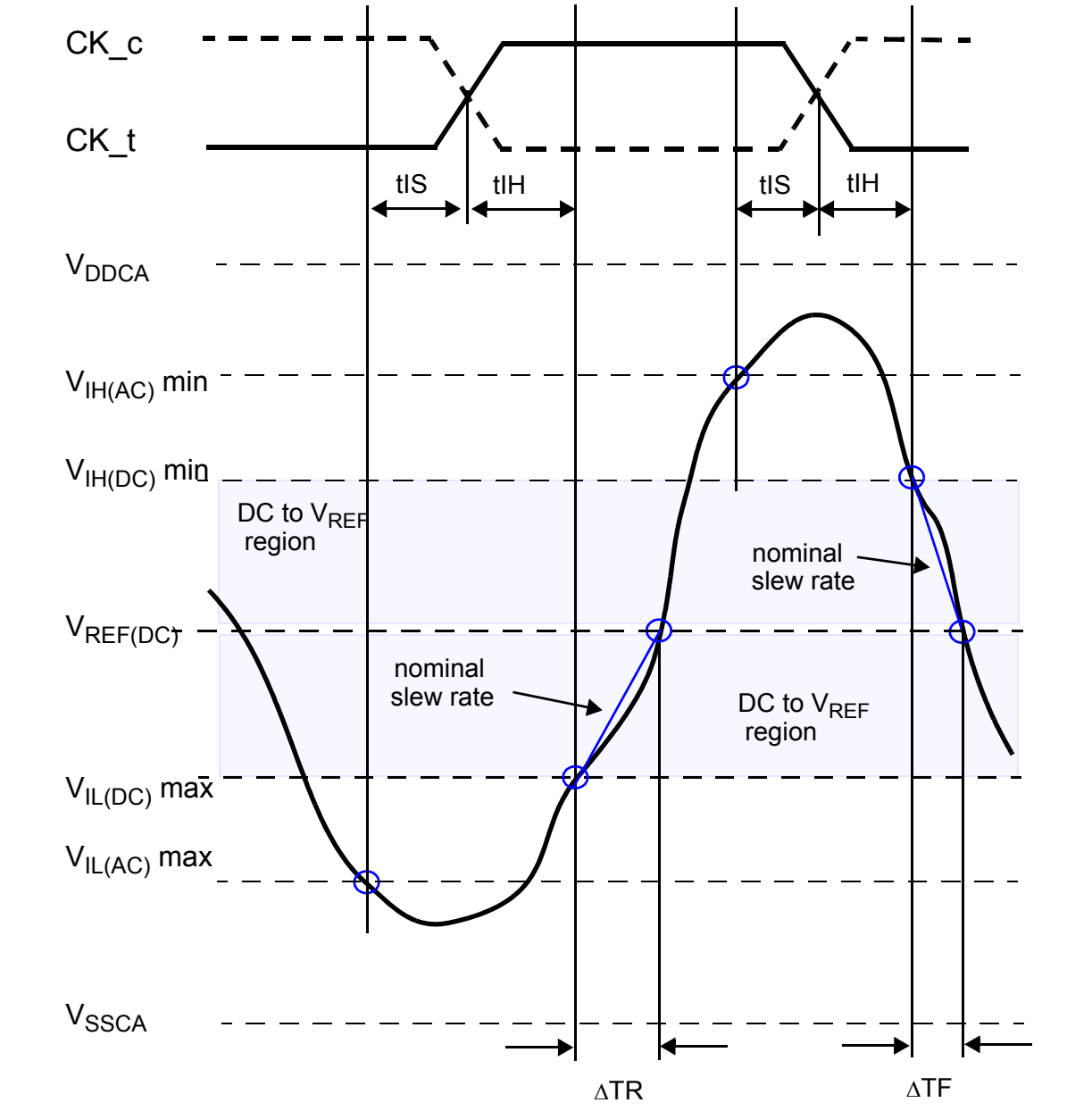
Slew Rate [V/ns]	t_{VAC} [ps] @150mV		t_{VAC} [ps] @150mV	
	1600Mbps		1333Mbps	
	MIN	MAX	MIN	MAX
> 4.0	48	-	58	-
4.0	48	-	58	-
3.5	46	-	56	-
3.0	43	-	53	-
2.5	40	-	50	-
2.0	35	-	45	-
1.5	27	-	37	-
<1.5	27	-	37	-



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(DC)} - V_{IL(AC)}max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(AC)}min - V_{REF(DC)}}{\Delta TR}$$

Figure. Illustration of nominal slew rate and t_{VAC} for setup time t_{IS} for CA and CS_n with respect to clock



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(DC)} - V_{IL(DC)}max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(DC)}min - V_{REF(DC)}}{\Delta TF}$$

Figure. Illustration of nominal slew rate for hold time tIH for CA and CS_n with respect to clock

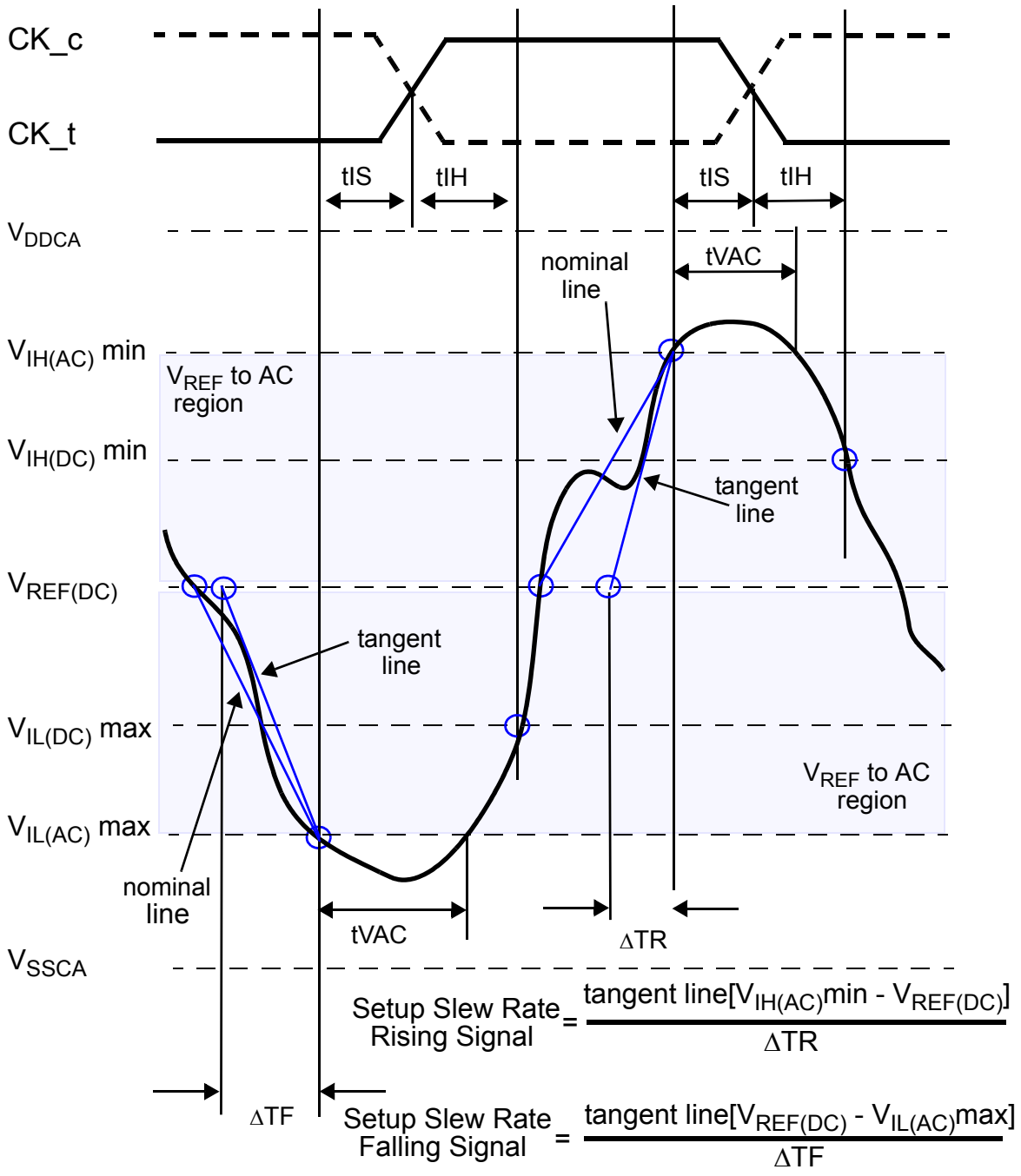
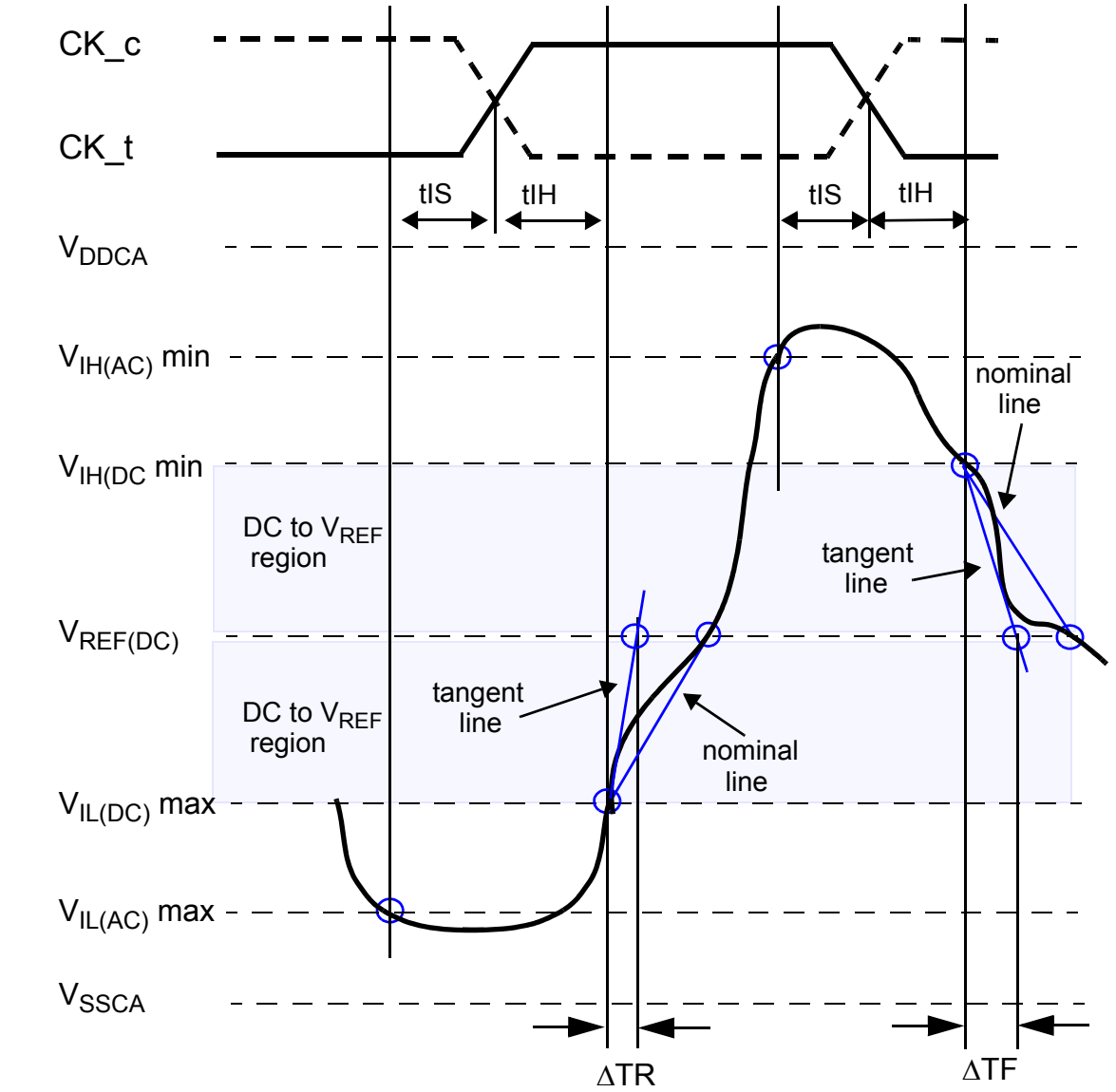


Figure. Illustration of tangent line for setup time t_{IS} for CA and CS_n with respect to clock



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(DC)}\text{max}]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [V_{IH(DC)}\text{min} - V_{REF(DC)}]}{\Delta TF}$$

Figure. Illustration of tangent line for hold time t_{IH} for CA and CS_n with respect to clock

Data Setup, Hold and Slew Rate Derating

For all input signals (DQ, DM) the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value to the ΔtDS and ΔtDH derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC)max. If the actual signal is always earlier than the nominal slew rate line between shaded `VREF(DC) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded `VREF(DC) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VREF(DC). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VREF(DC). If the actual signal is always later than the nominal slew rate line between shaded `dc level to VREF(DC) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded `dc to VREF(DC) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(DC) level is used for derating value.

For a valid transition the input signal has to remain above/below VIH/IL(AC) for some time tVAC.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(AC).

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

Table. Data Setup and Hold Base-Values

unit [ps]	LPDDR3 1600	LPDDR3 1333	Reference
tDS(base)	75	100	VIH/L(AC)=VREF(DC)+/-150mV
tDH(base)	100	125	VIH/L(DC)=VREF(DC)+/-100mV

Note 1: AC/DC referenced for 2V/ns DQ, DM slew rate and 4V/ns differential DQS_t-DQS_c slew rate.

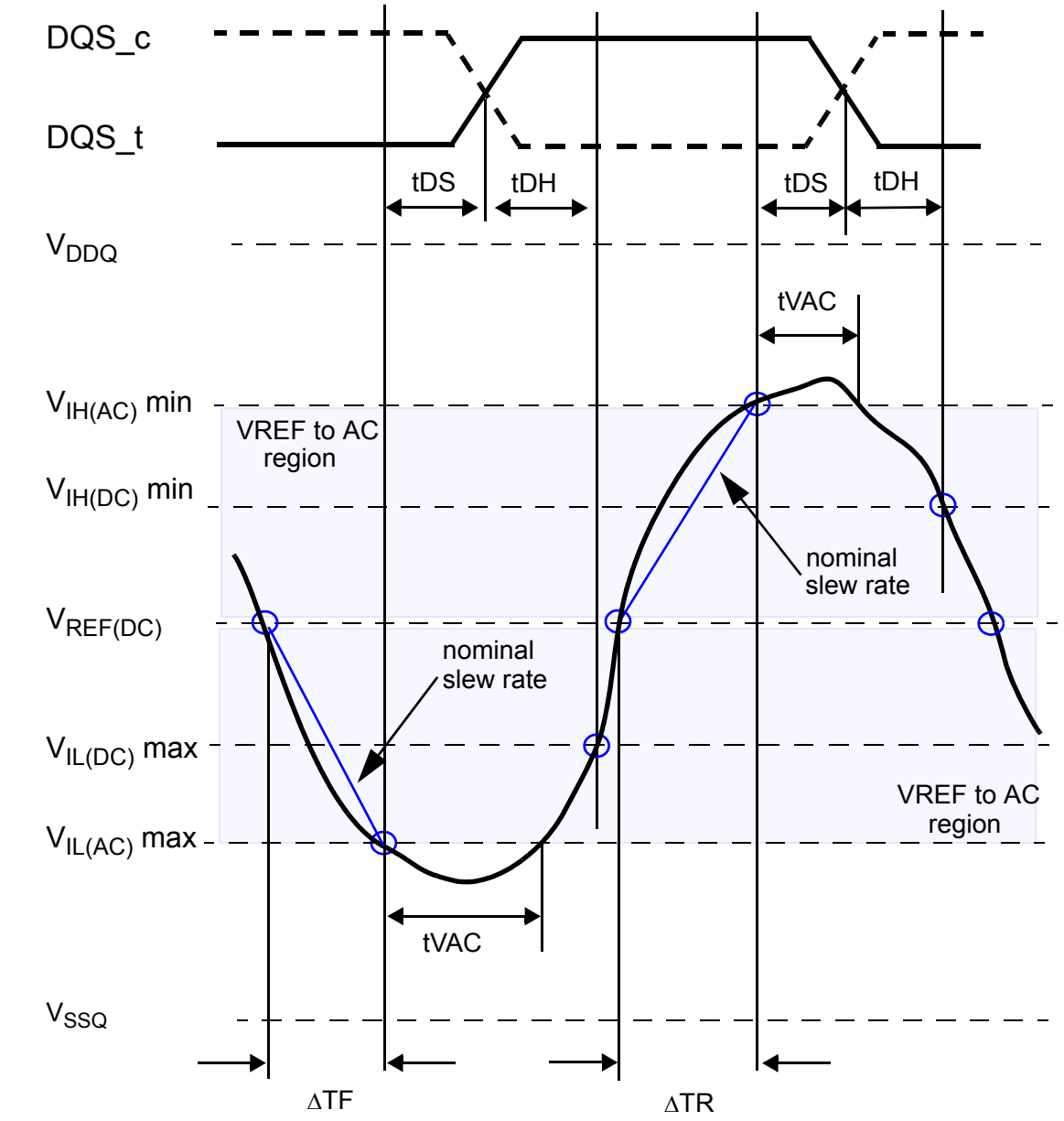
Table. Derating values LPDDR3 tDS/tDH - AC/DC based AC150

		ΔtDS, ΔtDH derating in [ps] AC/DC based AC150 Threshold -> VIH(ac)=VREF(dc)+150mV, VIL(ac)=VREF(dc)-150mV DC100 Threshold -> VIH(dc)=VREF(dc)+100mV, VIL(dc)=VREF(dc)-100mV											
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ,DM Slew rate V/ns	4.0	38	25	38	25	38	25						
	3.0			25	17	25	17	25	17	25	17	38	29
	2.0					0	0	0	0	0	0	13	13
	1.5							-25	-17	-25	-17	-12	-4

Note 1: Cell contents shaded in red are defined as 'not supported'

Table. Required time t_{VAC} above VIH(ac) {below VIL(ac)} for valid transition

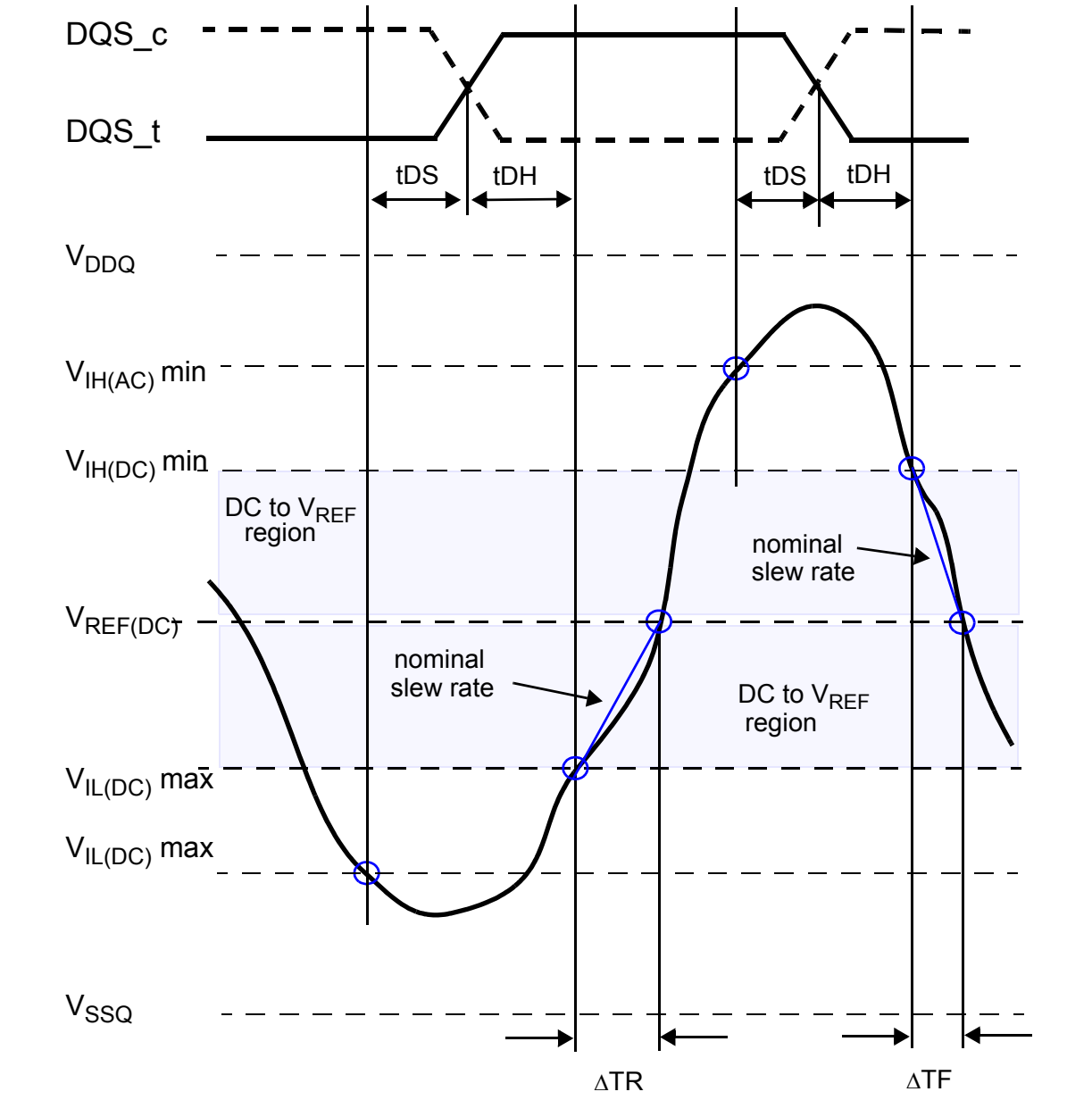
Slew Rate [V/ns]	t_{VAC} [ps] @150mV		t_{VAC} [ps] @150mV	
	1600Mbps		1333Mbps	
	MIN	MAX	MIN	MAX
> 4.0	48	-	58	-
4.0	48	-	58	-
3.5	46	-	56	-
3.0	43	-	53	-
2.5	40	-	50	-
2.0	35	-	45	-
1.5	27	-	37	-
<1.5	27	-	37	-



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(DC)} - V_{IL(AC)}max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(AC)}min - V_{REF(DC)}}{\Delta TR}$$

Figure. Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} for DQ with respect to strobe



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(DC)} - V_{IL(DC)}max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(DC)}min - V_{REF(DC)}}{\Delta TF}$$

Figure. Illustration of nominal slew rate for hold time t_{DH} for DQ with respect to strobe

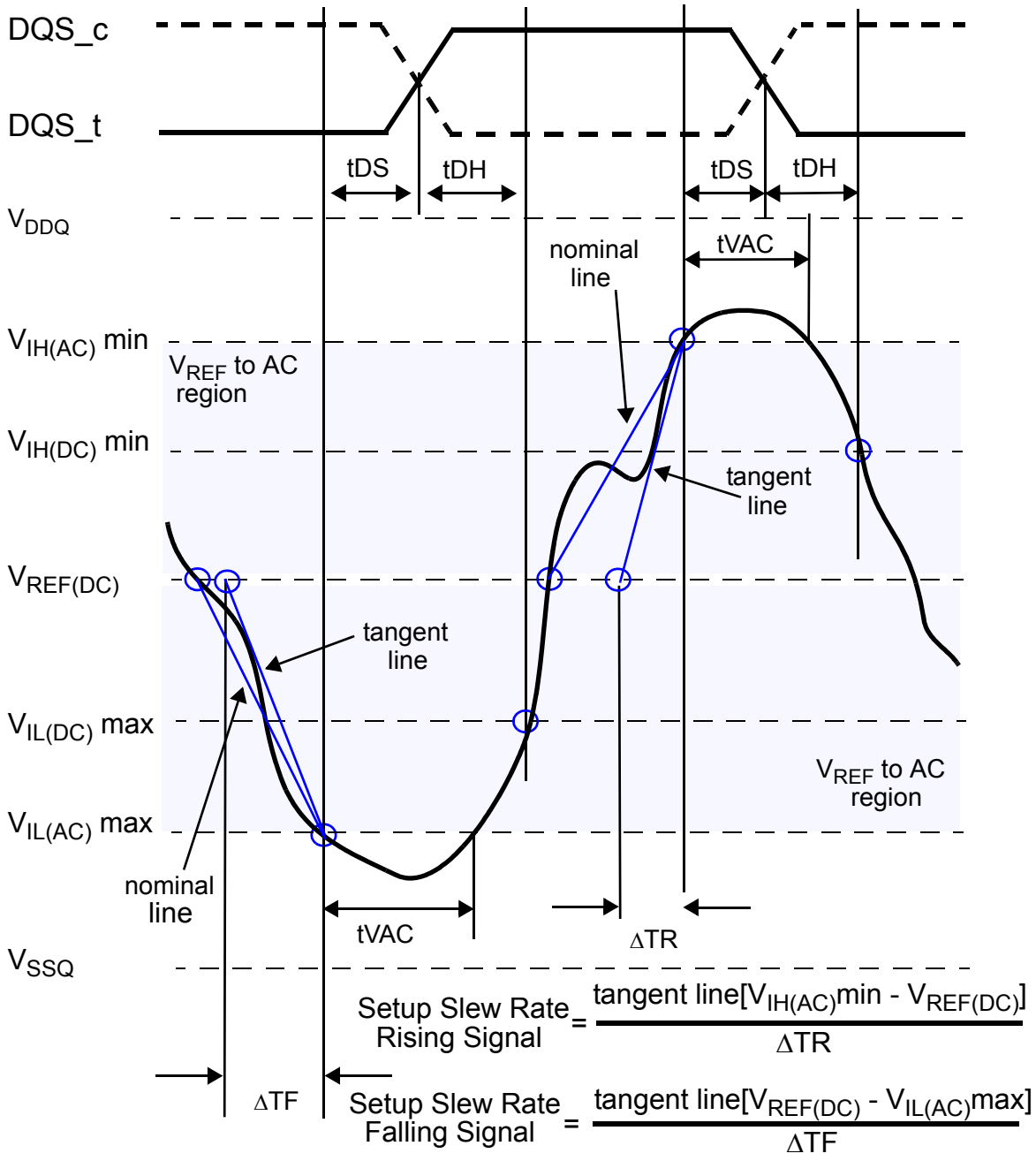
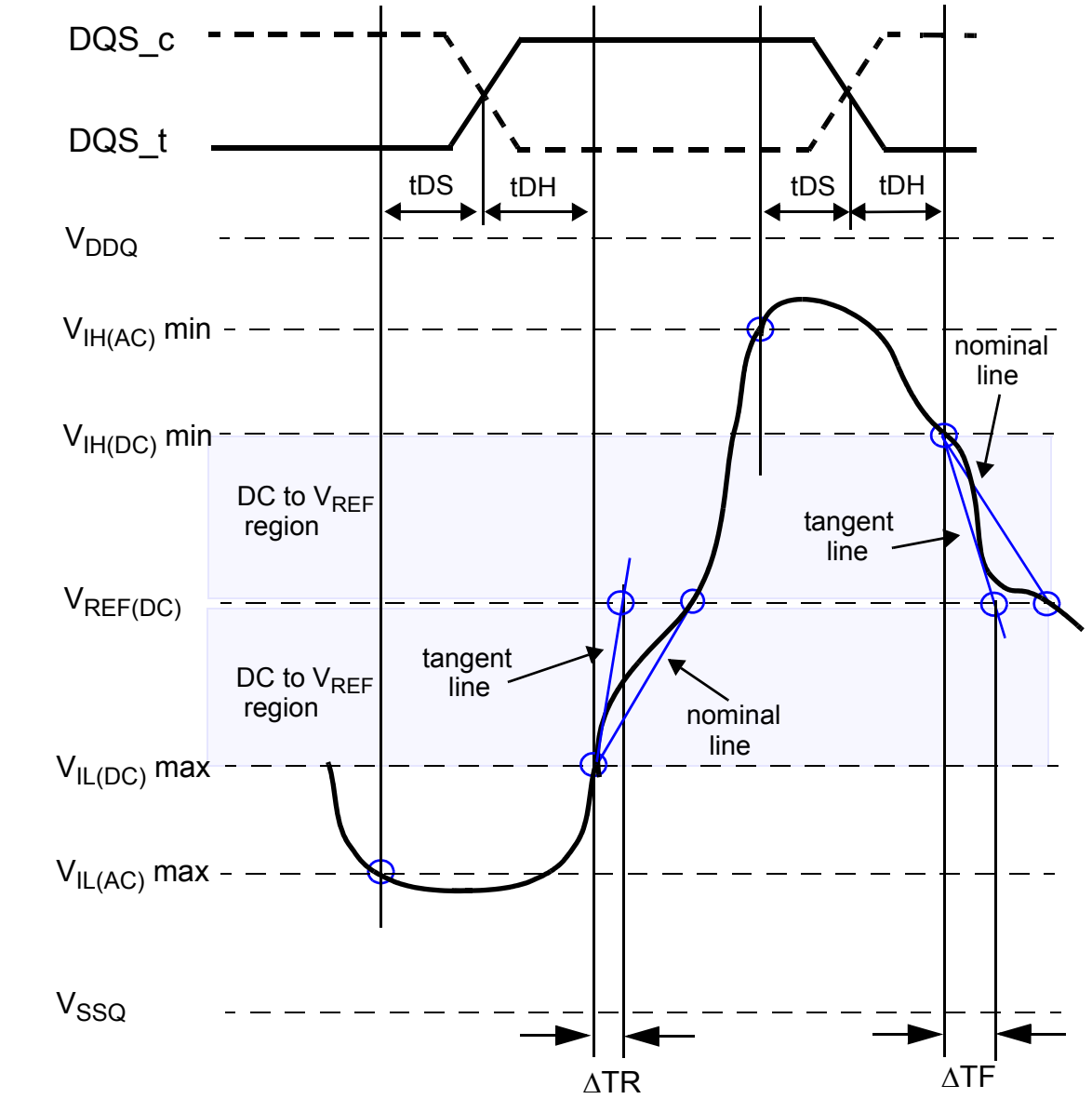


Figure. Illustration of tangent line for setup time t_{DS} for DQ with respect to strobe



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(DC)}\text{max}]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [V_{IH(DC)}\text{min} - V_{REF(DC)}]}{\Delta TF}$$

Figure. Illustration of tangent line for hold time t_{DH} for DQ with respect to strobe

Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR3 device.

Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j \right) / N$$
$$where \quad N = 200$$

Unit `tCK(avg)' represents the actual clock average tCK(avg) of the input clock under operation. Unit `nCK' represents one clock cycle of the input clock, counting the actual clock edges.

tCK(avg) may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specifications are met.

Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.

Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j \right) / (N \times tCK(avg))$$
$$where \quad N = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j \right) / (N \times tCK(avg))$$
$$where \quad N = 200$$

Definition for tJIT(per)

tJIT(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).
tJIT(per) = Min/max of {tCK_i - tCK(avg) where i = 1 to 200}. ?
tJIT(per),act is the actual clock jitter for a given system.?
tJIT(per),allowed is the specified allowed clock period jitter.?
tJIT(per) is not subject to production test.

Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.
tJIT(cc) = Max of |{tCK_{i+1} - tCK_i}|. ?
tJIT(cc) defines the cycle to cycle jitter.?
tJIT(cc) is not subject to production test.

Definition for tERR(nper)

tERR(nper) is defined as the cumulative error across n multiple consecutive cycles from tCK(avg).
tERR(nper),act is the actual clock jitter over n cycles for a given system.?
tERR(nper),allowed is the specified allowed clock period jitter over n cycles.?
tERR(nper) is not subject to production test.

$$tERR(nper) = \left(\sum_{j=i}^{i+n-1} tCK_j \right) - n \times tCK(avg)$$

tERR(nper),min can be calculated by the formula shown below:

$$tERR(nper), min = (1 + 0.68\,LN(n)) \times tJIT(per), min$$

tERR(nper),max can be caculated by the formula shown below:

$$tERR(nper), max = (1 + 0.68\,LN(n)) \times tJIT(per), max$$

Using these equations, tERR(nper) tables can be generated for each tJIT(per),act value

Definition for duty cycle jitter tJIT(duty)

tJIT(duty) is defined with absolute and average specification of tCH / tCL.

tJIT(duty),min can be caculated by the formula shown below:

$$tJIT(duty),min = MIN((tCH(abs),min - tCH(avg),min),(tCL(abs),min - tCL(avg),min)) \times tCK(avg)$$

tJIT(duty),max can be caculated by the formula shown below:

$$tJIT(duty),max = MAX((tCH(abs),max - tCH(avg),max),(tCL(abs),max - tCL(avg),max)) \times tCK(avg)$$

Definition for tCK(abs), tCH(abs) and tCL(abs)

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

Parameter	Symbol	Min	Unit
Absolute Clock Period	tCK(abs)	tCK(avg),min + tJIT(per),min	ps
Absolute Clock HIGH Pulse Width	tCH(abs)	tCH(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)
Absolute Clock LOW Pulse Width	tCL(abs)	tCL(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)

Note:
1. tCK(avg),min is expressed in ps for this table
2. tJIT(duty),min is a negative value

Period Clock Jitter

LPDDR3 devices can tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter (tJIT(per)) in excess of the values found in "AC timing table" and how to determine cycle time de-rating and clock cycle de-rating.

Clock period jitter effects on core timing parameters
(tRCD, tRP, tRTP, tWR, tWRA, tWTR, tRC, tRAS, tRRD, tFAW)

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR3 device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}.

When the device is operated with clock jitter outside specification limits, the number of clocks or tCK(avg) may need to be increased based on the values for each core timing parameter.

Cycle time de-rating for core timing parameters

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the amount of cycle time de-rating (in ns) required if the equation results in a positive value for a core timing parameter (tCORE).

$$Cycle\ Time\ Derating = MAX\left\{\left(\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tnPARAM} - tCK(avg)\right), 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

Clock Cycle de-rating for core timing parameters

For a given number of clocks (tnPARAM) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter (tJIT(per)).
For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter (tCORE).

$$ClockCycleDerating = RU\left\{\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tCK(avg)}\right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

Clock jitter effects on Command/Address timing parameters
(tIS, tIH, tISCKE, tIHCKE, tISb, tIHb, tISCKEb, tIHCKEb)

These parameters are measured from a command/address signal (CKE, CS, CA0 - CA9) transition edge to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

Clock jitter effects on Read timing parameters

tRPRE

When the device is operated with input clock jitter, tRPRE needs to be de-rated by the actual period jitter (tJIT(per),act,max) of the input clock in excess of the allowed period jitter (tJIT(per),allowed,max). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9 - \left(\frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)}\right)$$

For example,
if the measured jitter into a LPDDR3-1600 device has tCK(avg) = 1250 ps, tJIT(per),act,min = -92 ps and tJIT(per),act,max = + 134 ps, then,
tRPRE,min,derated = 0.9 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg)
= 0.9 - (134 - 100)/1250= .8728 tCK(avg)

tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal (DMn, DQm: n=0,1,2,3, m=0-31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. tJIT(per)).

tQSH, tQSL

These parameters are affected by duty cycle jitter which is represented by tCH(abs)min and tCL(abs)min. These parameters determine absolute Data-Valid Window (DVW) at the LPDDR3 device pin.
Absolute min DVW @ LPDDR3 device pin =
min{ (tQSH(abs)min – tDQSQmax) , (tQSL(abs)min – tDQSQmax) }
This minimum DVW shall be met at the target frequency regardless of clock jitter.

tRPST

tRPST is affected by duty cycle jitter which is represented by tCL(abs). Therefore tRPST(abs)min can be specified by tCL(abs)min.
tRPST(abs)min = tCL(abs)min – 0.05 = tQSL(abs)min

Clock jitter effects on Write timing parameters

tDS, tDH

These parameters are measured from a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition edge to its respective data strobe signal (DQSn_t, DQSn_c : n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the data strobe signal crossing that latches the data. Regardless of clock jitter values, these values shall be met.

tDSS, tDSH

These parameters are measured from a data strobe signal (DQSx_t, DQSx_c) crossing to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold of the data strobes are relative to the corresponding clock signal crossing. Regardless of clock jitter values, these values shall be met.

tDQSS

This parameter is measured from a data strobe signal (DQSx_t, DQSx_c) crossing to the subsequent clock signal (CK_t/CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual period jitter tJIT(per),act of the input clock in excess of the allowed period jitter tJIT(per),allowed.

tDQSS(min,derated) can be caculated by the formula shown below:

$$tDQSS(min, derated) = 0.75 - \frac{tJIT(per), act,min - tJIT(per),allowed,min}{tCK(avg)}$$

tDQSS(max,derated) can be caculated by the formula shown below:

$$tDQSS(max, derated) = 1.25 - \frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)}$$

For example,
if the measured jitter into a LPDDR3-1600 device has
tCK(avg)= 1250 ps, tJIT(per),act,min= -93 ps and tJIT(per),act,max= + 134 ps, then
tDQSS,(min,derated) = 0.75 - (tJIT(per),act,min - tJIT(per),allowed,min)/tCK(avg) = 0.75 - (-93 + 100)/1250 = 0.7444 tCK(avg)
and
tDQSS,(max,derated) = 1.25 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 1.25 - (134 - 100)/1250 = 1.2228 tCK(avg)

Refresh Requirements

Density		Symbol	4Gb	Unit
Number of Banks			8	-
Refresh Window Tcase <= 85'C		tREFW	32	ms
Refresh Window 1/2-Rate Refresh		tREFW	16	ms
Refresh Window 1/4-Rate Refresh		tREFW	8	ms
Required number of REFRESH commands (min)		R	8,192	-
average time between REFRESH commands (for reference only) Tcase <= 85'C	REFab	tREFI	3.9	us
	REFpb	tREFIpb	0.4875	us
Refresh Cycle time		tRFCab	130	ns
Per Bank Refresh Cycle time		tRFCpb	60	ns

LPDDR3 Read and Write Latencies

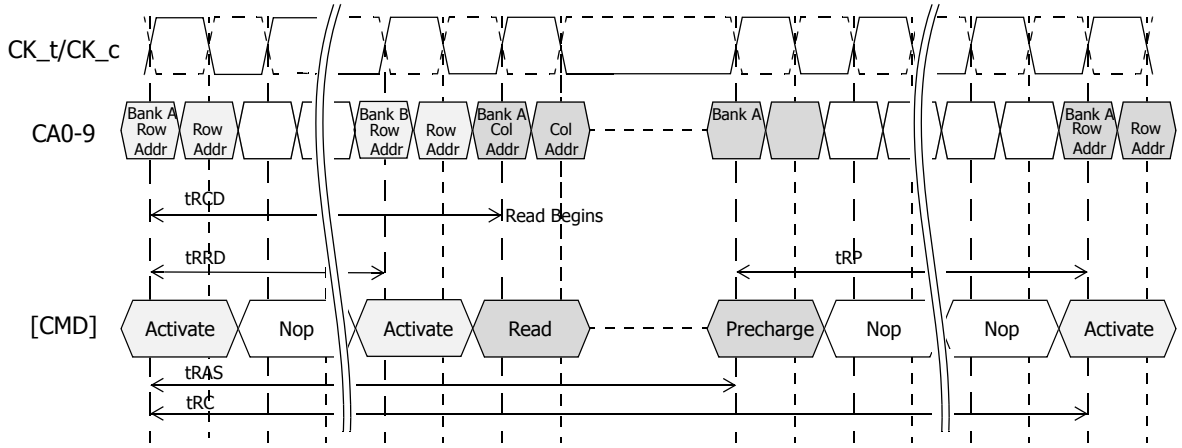
Parameter	LPDDR3							Unit
	333	800	1066	1200	1333	1466	1600	
Max. Clock Frequency	166	400	533	600	667	733	800	NHz
Max. Data Rate	333	800	1066	1200	1333	1466	1600	MT/s
Average Clock Period	6	2.5	1.875	1.667	1.5	1.364	1.25	ns
Read Latency	3[1]	6	8	9	10	11	12	tCK(avg)
Write Latency (Set A)	1[1]	3	4	5	6	6	6	tCK(avg)
Write Latency (Set B)	1[1]	3	4	5	8	9	9	tCK(avg)

Note:
1. RL=3/WL=1 setting is an optional feature. Refer to MR0 OP<7>.
2. Write Latency (Set B) support is an optional feature. Refer to MR0 OP<6>.

Command Definitions

Activate command

The ACTIVATE command is issued by holding CS_n LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA0 to BA2 are used to select the desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at tRCD after the ACTIVATE command is issued. After a bank has been activated it must be precharged before another ACTIVATE command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive ACTIVATE commands to the same bank is determined by the RAS cycle time of the device (tRC). The minimum time interval between ACTIVATE commands to different banks is tRRD.



Note:
1. A PRECHARGE-all command uses tRPab timing, while a single-bank PRECHARGE command uses tRPpb timing. In this figure, tRP is used to denote either an all-bank PRECHARGE or a single-bank PRECHARGE.

Figure. Activate command

Certain restrictions on operation of the 8-bank LPDDR3 devices must be observed. There are two rules: One rule restricts the number of sequential ACTIVATE commands that can be issued; the other provides more time for RAS precharge for a PRECHARGE ALL command. The rules are as follows:

- 8 bank device Sequential Bank Activation Restriction: No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. The number of clocks in a tFAW period is dependent upon the clock frequency, which may vary. If the clock frequency is not changed over this period, converting clocks is done by dividing tFAW[ns] by tCK[ns], and rounding up to the next integer value. As an example of the rolling window, if RU(tFAW/tCK) is 10 clocks, and an ACTIVATE command is issued in clock n, no more than three further ACTIVATE commands can be issued at or between clock n + 1 and n + 9. REFpb also counts as bank activation for purposes of tFAW. If the clock frequency is changed during the tFAW period, the rolling tFAW window may be calculated in clock cycles by adding up the time spent in each clock period. The tFAW requirement is met when the previous n clock cycles exceeds the tFAW time.

- 8 bank device Precharge All Allowance: tRP for a PRECHRGE ALL command must equal tRPab, which is greater than tRPpb.

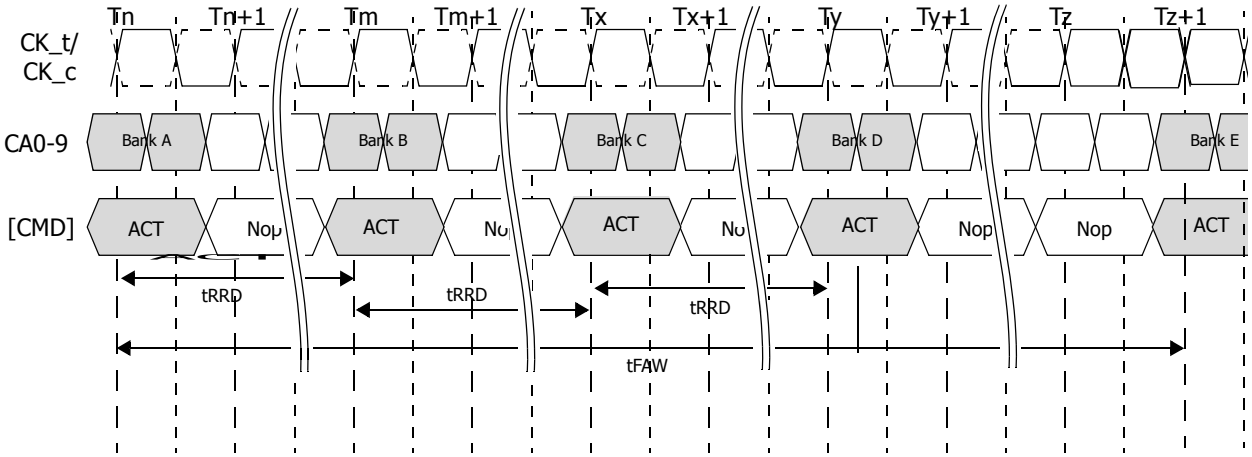
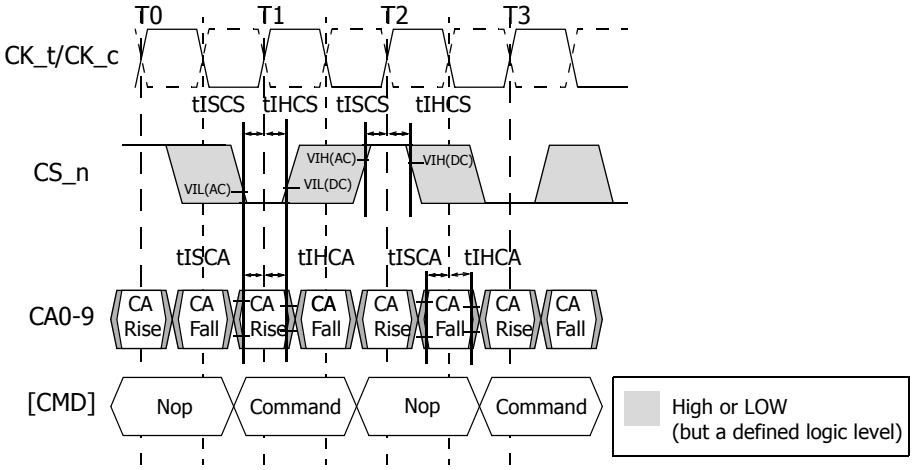


Figure. tFAW timing

Command Input Setup and Hold Timing

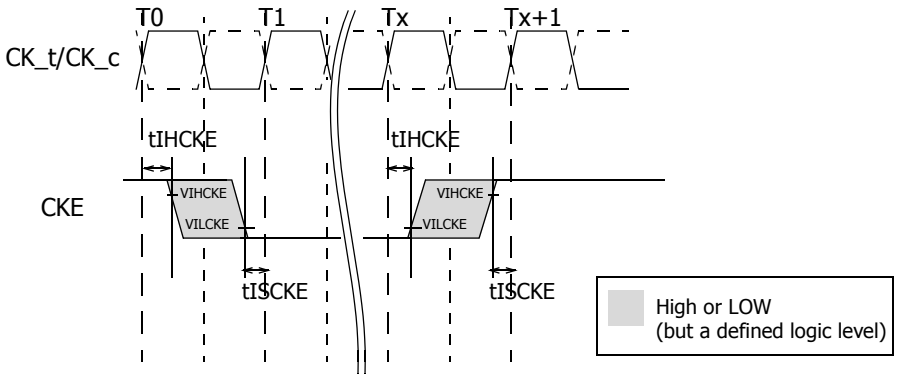


Note:

1. Setup and hold conditions also apply to the CKE pin. See section related to power down for timing diagrams related to the CKE pin.

Figure. Command Input Setup and Hold timing

CKE Input Setup and Hold Timing



Note:
1. After CKE is registered LOW, CKE signal level shall be maintained below VILCKE for tCKE specification (LOW pulse width).
2. After CKE is registered HIGH, CKE signal level shall be maintained above VIHCKE for tCKE specification (HIGH pulse width).

Figure. CKE Input Setup and Hold timing

Read and Write access modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting CS_n LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a read operation (CA2 HIGH) or a write operation (CA2 LOW).
The LPDDR3 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles.
(optional) Reads may be interrupted by Reads and Writes may be interrupted by Writes provided that this occurs on even clock cycles after the Read or Write command and tCCD is met. The Minimum CAS to CAS delay is defined by tCCD.

Burst read command

The burst READ command is initiated with CS_n LOW, CA0 HIGH, CA1 LOW, and CA2 HIGH at the rising edge of the clock. The command address bus inputs CA5r–CA6r and CA1f–CA9f determine the starting column address for the burst. The read latency (RL) is defined from the rising edge of the clock on which the READ command is issued to the rising edge of the clock from which the tDQSCK delay is measured. The first valid data is available RL × tCK + tDQSCK + tDQSQ after the rising edge of the clock when the READ command is issued. The data strobe output is driven LOW tRPRE before the first valid rising strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin, edge-aligned with the data strobe. The RL is programmed in the mode registers. Pin timings for the data strobe are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

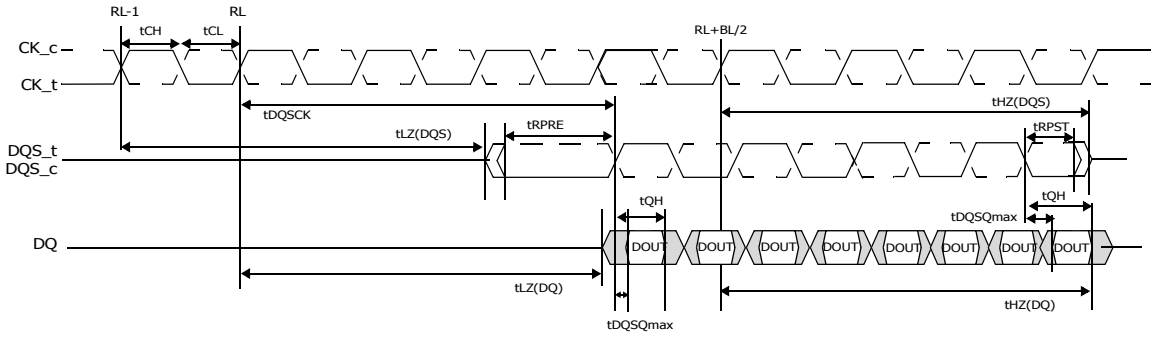


Figure. Read Output Timing

Note:
1. tDQSCK can span multiple clock periods.
2. An effective Burst Length of 8 is shown.

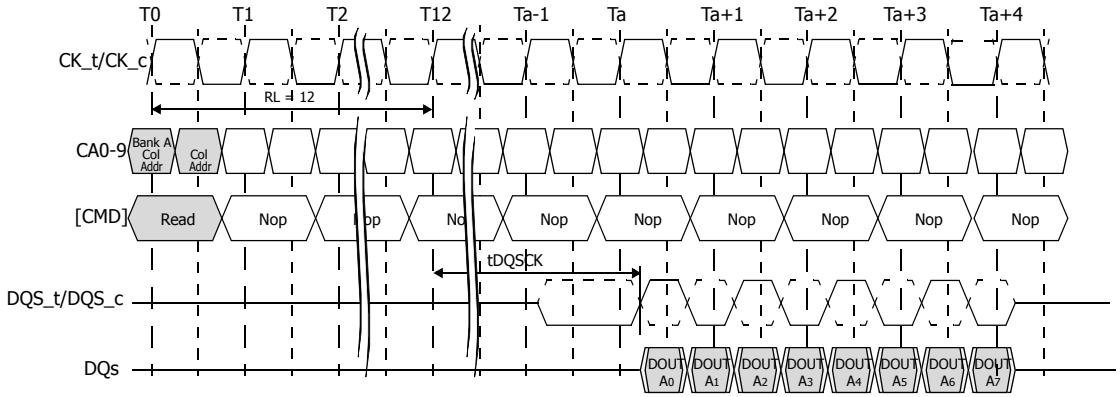


Figure. Burst Read : RL=12, BL=8, tDQSCK>tCK

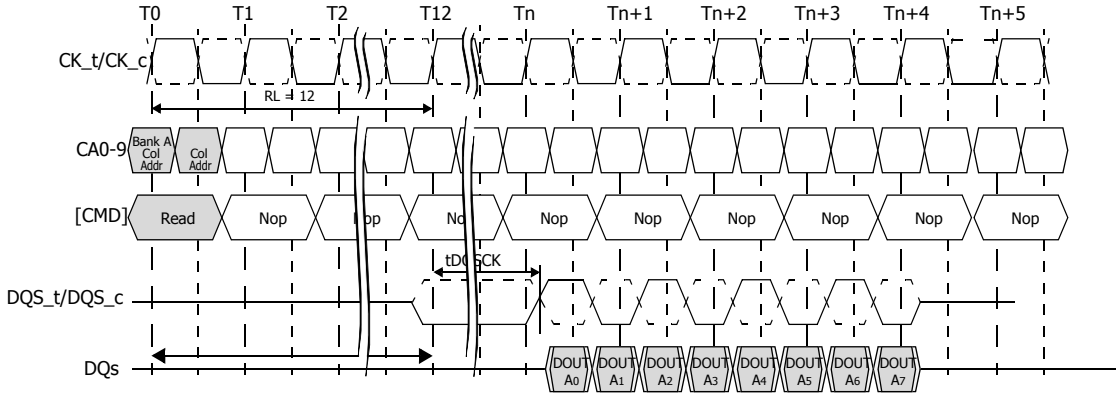


Figure. Burst Read : RL=12, BL=8, tDQSCK<tCK

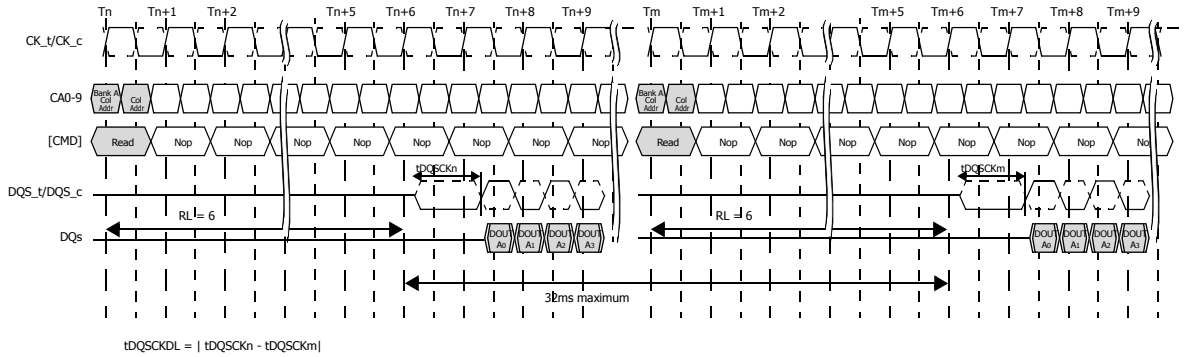


Figure. LPDDR3 : tDQSCKDL timing

Note:

1. tDQSCKDLmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn ,tDQSCKm} pair within any 32ms rolling window.

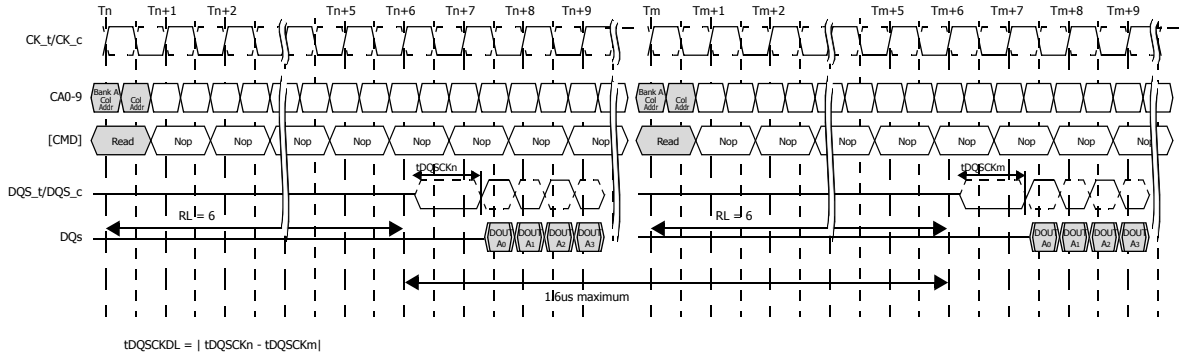


Figure. LPDDR3 : tDQSCKDM timing

Note:

1. tDQSCKDMmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn ,tDQSCKm} pair within any 1.6us rolling window.

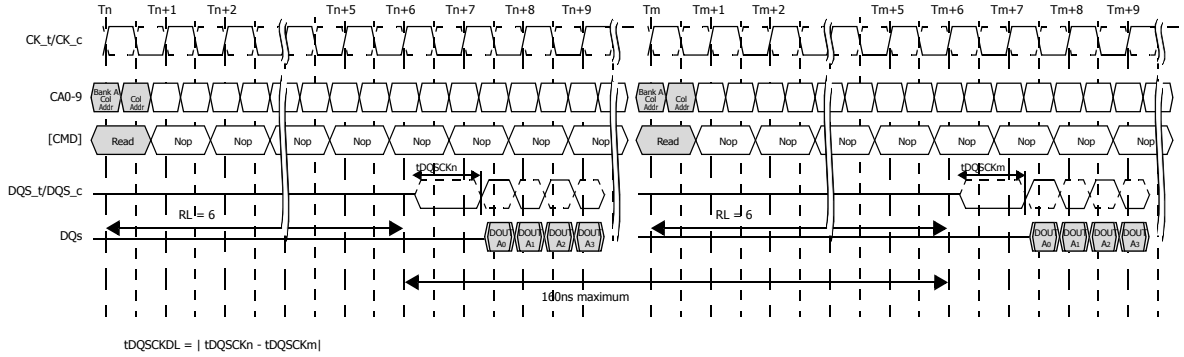


Figure. LPDDR3 : tDQSCKDS timing

Note:

1. tDQSCKDSmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn ,tDQSCKm} pair within any 160ns rolling window.

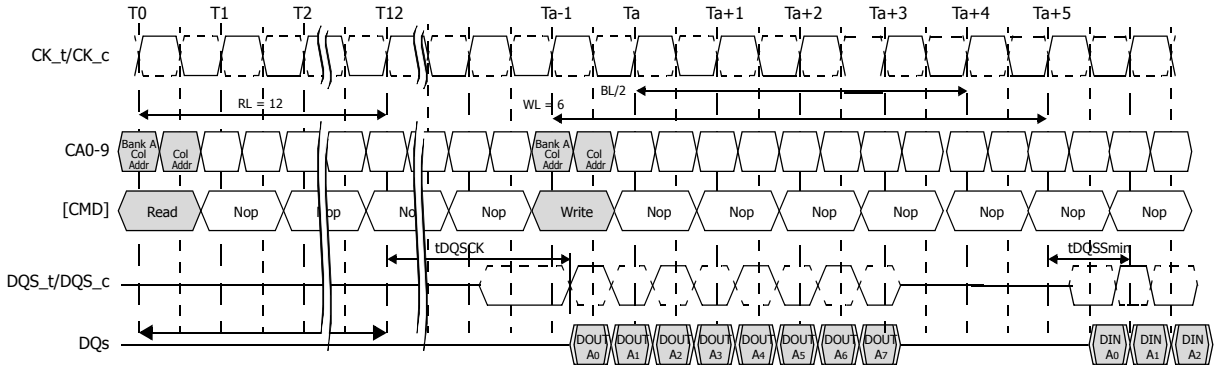


Figure. Burst READ Followed by Burst WRITE: RL=12, WL=6, BL=8

The minimum time from the burst READ command to the burst WRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE latency is RL + RU(tDQSCK(MAX)/tCK) + BL/2 + 1 - WL clock cycles.

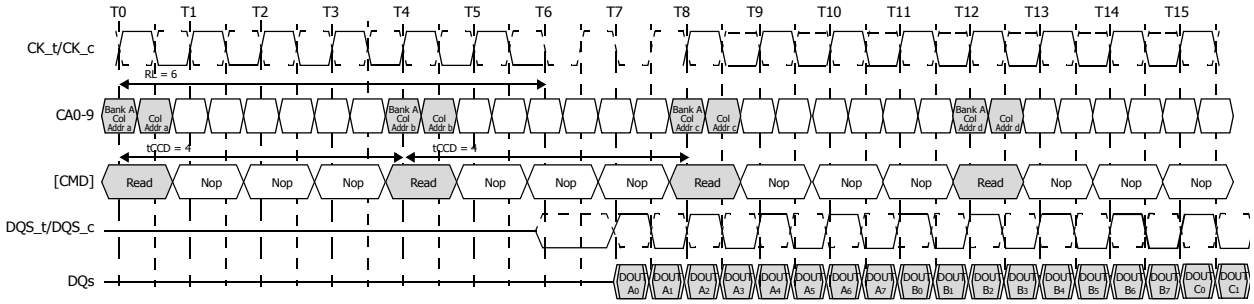
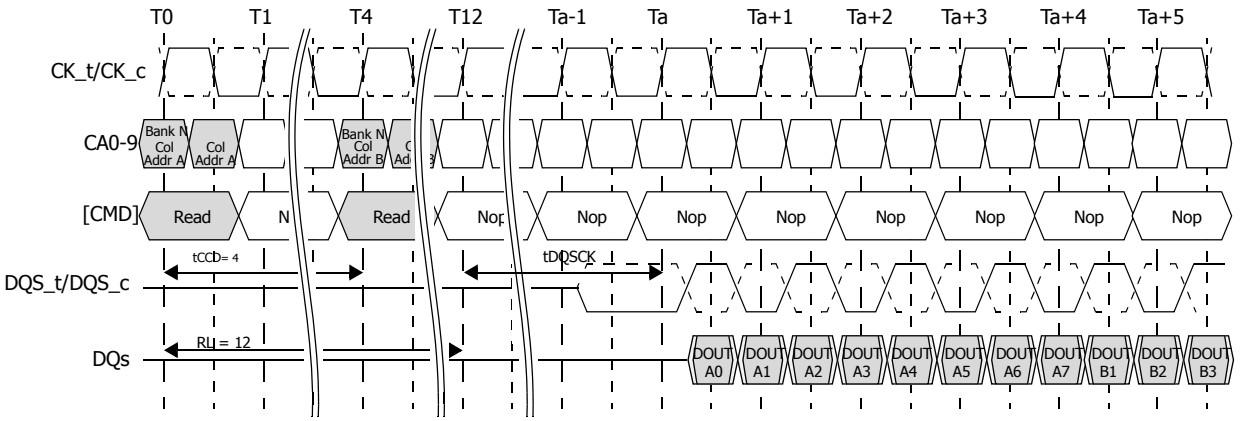


Figure. Seamless Burst READ: RL = 6, BL = 8, tCCD = 4

The seamless burst READ operation is supported by enabling a READ command at every fourth clock cycle for BL = 8 operation. This operation is supported as long as the banks are activated, whether the accesses read the same or different banks.

Reads interrupted by a read (optional)

Burst read can be interrupted by another read on even clock cycles after the Read command, provided that tCCD is met.



Note:

1. Read burst interrupt function is only allowed on burst of 16.
2. Read burst interrupt may only occur on 4 clock cycles after the previous read commands, provided that tCCD is met.
3. Reads can only be interrupted by other reads or the BST command.
4. Read burst interruption is allowed to any bank inside DRAM.
5. Read burst with Auto-Precharge is not allowed to be interrupted.
6. The effective burst length of the first read equals two times the number of clock cycles between the first read and the interrupting read.

Figure. Read burst interrupt

Burst write operation

The burst WRITE command is initiated with CS_n LOW, CA0 HIGH, CA1 LOW, and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst. Write latency (WL) is defined from the rising edge of the clock on which the WRITE command is issued to the rising edge of the clock from which the tDQSS delay is measured. The first valid data must be driven WL × tCK + tDQSS from the rising edge of the clock from which the WRITE command is issued. The data strobe signal (DQS) must be driven for time tWPRE prior to data input. The burst cycle data bits must be applied to the DQ pins tDS prior to the associated edge of the DQS and held valid until tDH after that edge. Burst data is sampled on successive edges of the DQS until the 8-bit burst length is completed. After a burst WRITE operation, tWR must be satisfied before a PRE-CHARGE command to the same bank can be issued. Pin input timings are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

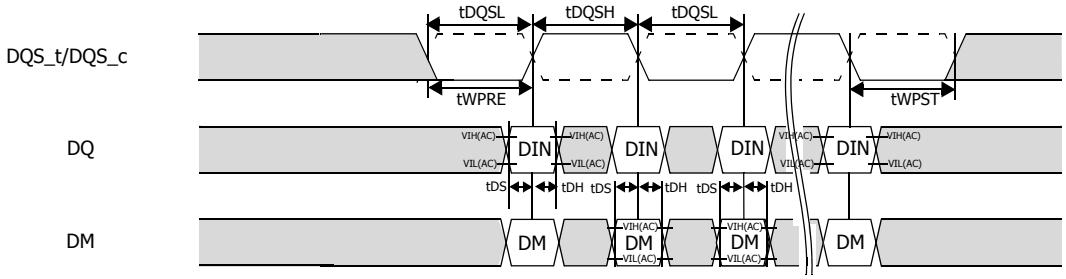


Figure. Data input (Write) timing

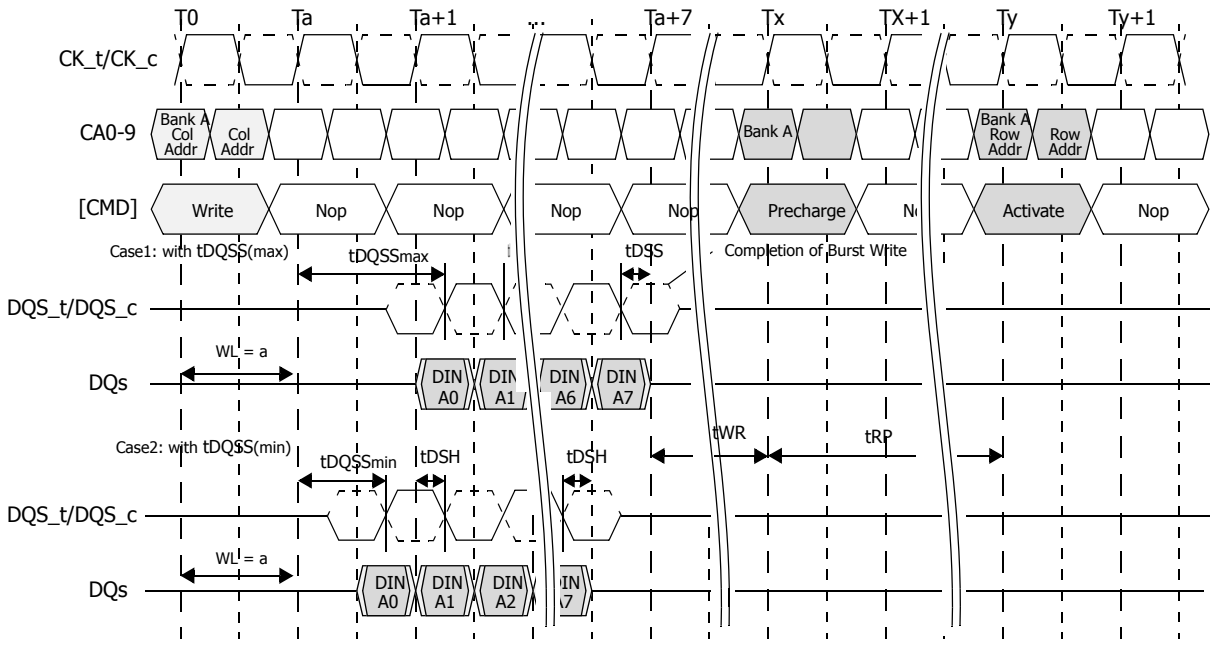


Figure. Burst write

tWPRE Calculation

The method for calculating tWPRE is shown in the following figure.

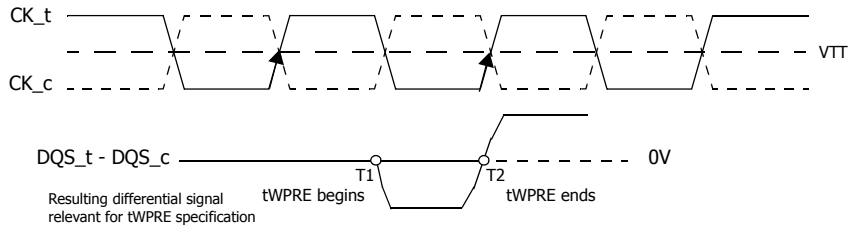


Figure. Method for Caculating tWPRE Transitions and Endpoints

tWPST Calculation

The method for calculating tWPST is shown in the following figure.

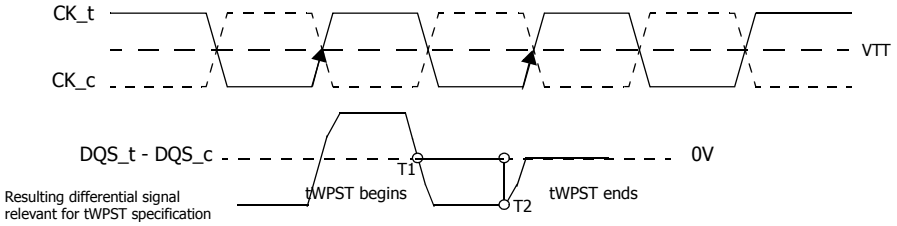
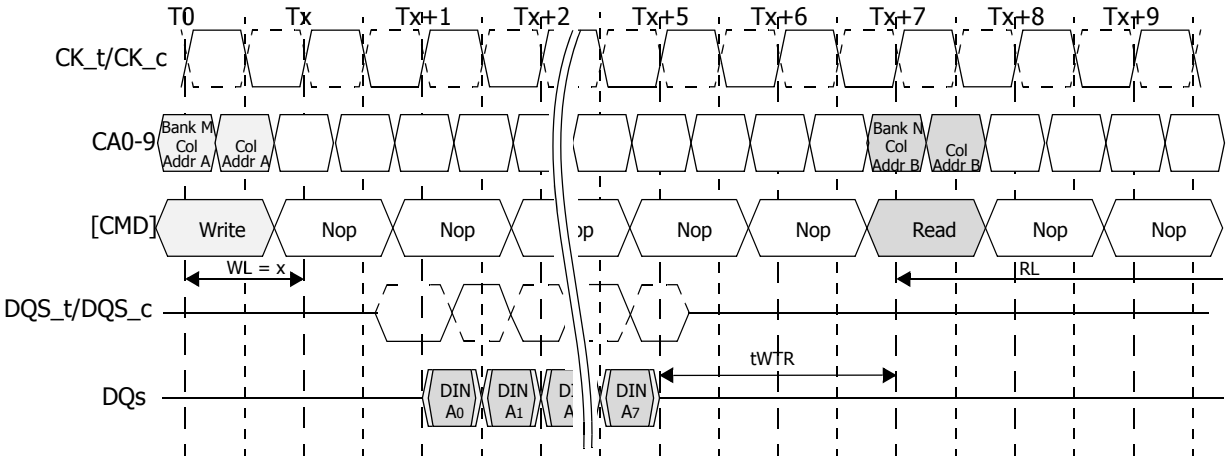


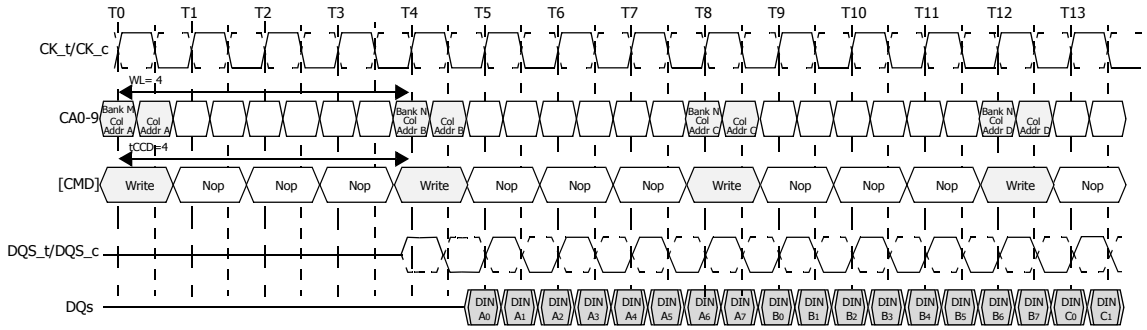
Figure. Method for Caculating tWPRE Transitions and Endpoints



Note:

1. The minimum number of clock cycles from the burst WRITE command to the burst READ command for any bank is [WL + 1 + BL/2 + RU(tWTR/tCK)].
2. tWTR starts at the rising edge of the clock after the last valid input data.

Figure. Burst write followed by burst Read



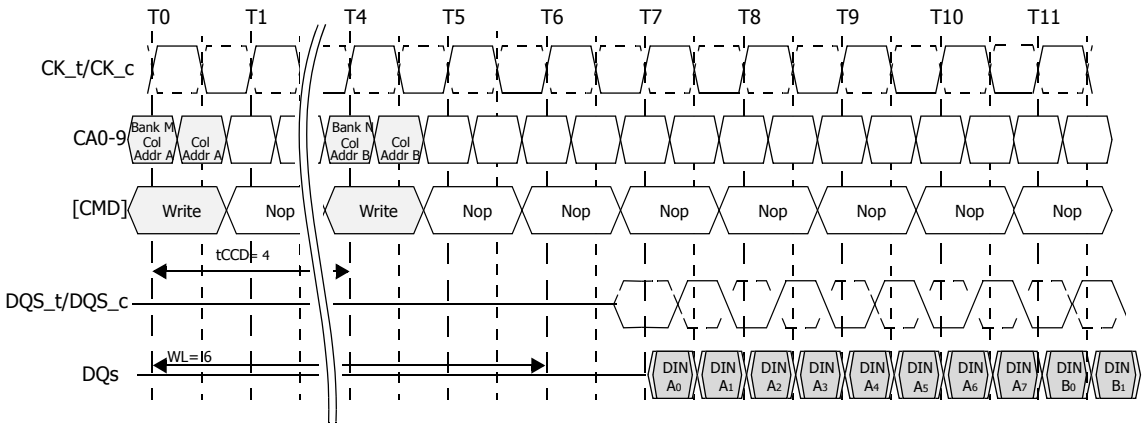
Note:

1. The seamless burst WRITE operation is supported by enabling a write command every four clocks for BL = 8 operation. This operation is supported for any activated bank.

Figure. Seamless Burst WRITE

Writes interrupted by a Write (optional)

Burst write can only be interrupted by another write on even clock cycles after the Write command, provided that tCCD(min) is met.



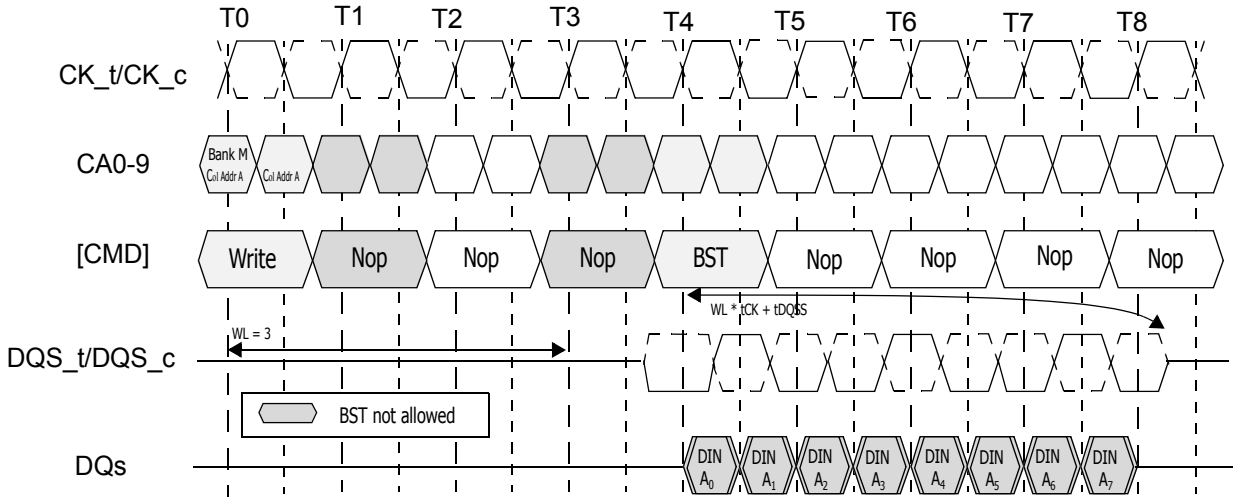
Note:

1. Write burst interrupt function is only allowed on burst of 16.
2. Write burst interrupt may only occur on 4 clock cycles after the previous write commands, provided that tCCD(min) is met.
3. Writes can only be interrupted by other writes or the BST command.
4. Write burst interruption is allowed to any bank inside DRAM.
5. Write burst with Auto-Precharge is not allowed to be interrupted.
6. The effective burst length of the first write equals two times the number of clock cycles between the first write and the interrupting write.

Figure. Write burst interrupt timing

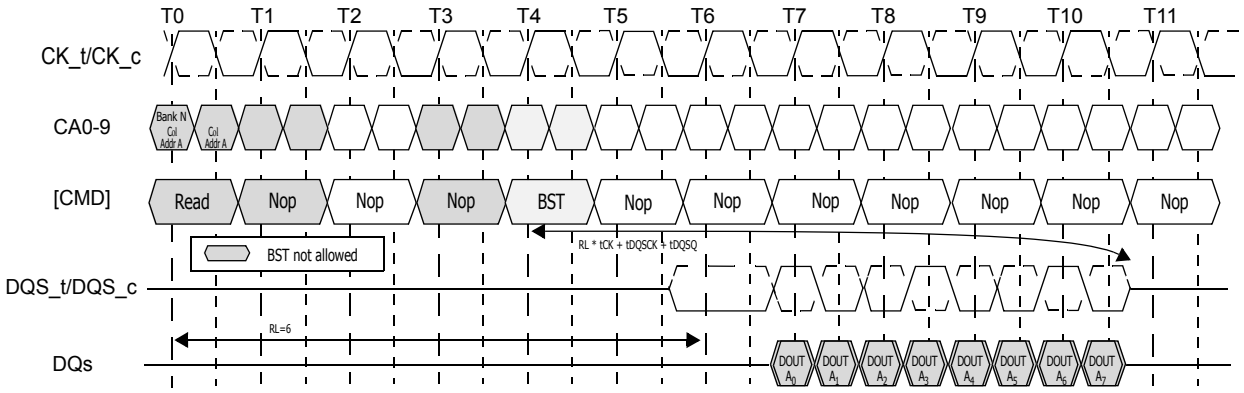
Burst Terminate (optional)

The Burst Terminate (BST) command is initiated by having CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of clock. A Burst Terminate command may only be issued to terminate an active Read or Write burst. Therefore, a Burst Terminate command may only be issued 4 clock cycles after a Read or Write command. The effective burst length of a Read or Write command truncated by a BST command is 8.
Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length(8) of the truncated burst should be used as "BL" to calculate the minimum read to write or write to read delay.
The BST command only affects the most recent read or write command. The BST command truncates an ongoing read burst RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Burst Terminate command is issued.
The BST command truncates an on going write burst WL * tCK + tDQSS after the rising edge of the clock where the Burst Terminate command is issued.
For LPDDR3 devices, the 8-bit prefetch architecture allows the BST command to be issued on an even number of clock cycles after a Write or Read command. Therefore, the effective burst length of a Read or Write command truncated by a BST command is an interger multiple of 8.



Note:
1. The BST command truncates an on going write burst WL *tCK + tDQSS after the rising edge of the clock where the Burst Terminate command is issued.
2. BST can only be issued 4 clock cycles after the Write command.
3. Additional BST commands are not allowed after Tx+3 and may not be issued until after the next Read or Write command.

Figure. Burst Write truncated by BST



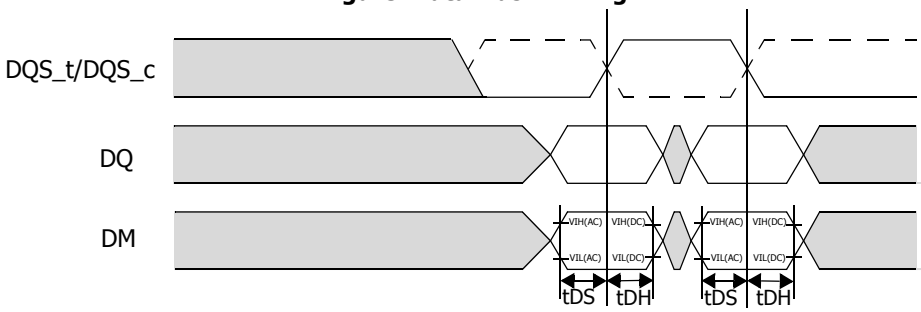
Note.
1. The BST command truncates an on going read burst RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Burst Terminate command is issued.
2. BST can only be issued 4 clock cycles after the Read command.
3. Additional BST commands are not allowed after Tx+1 and may not be issued until after the next Read or Write command.

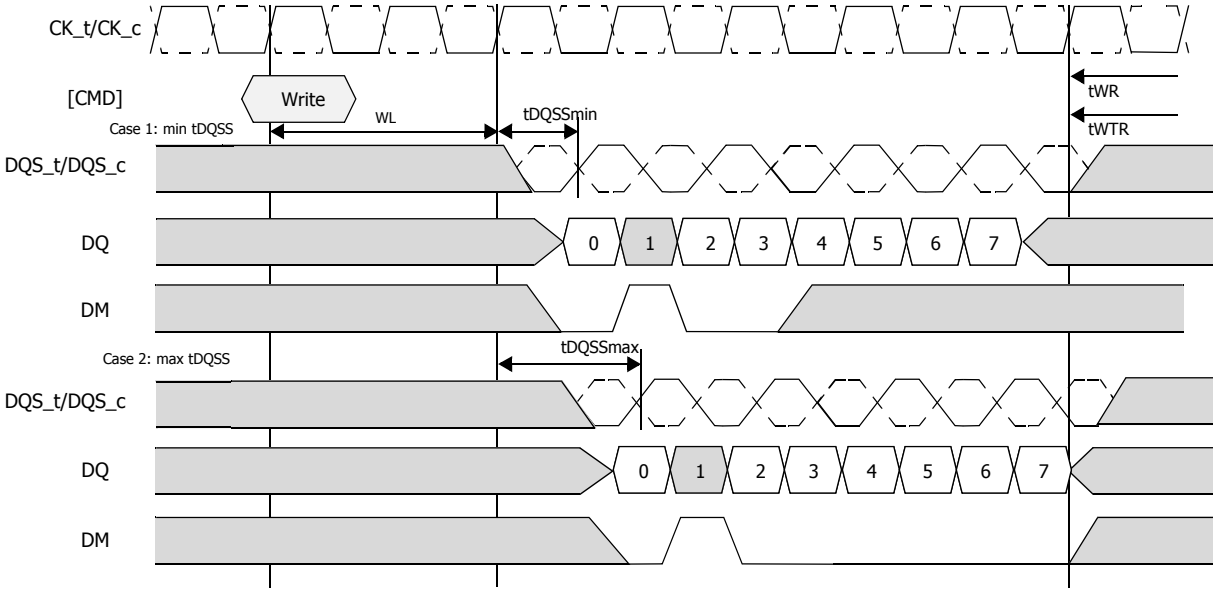
Figure. Burst Read truncated by BST

Write data mask

One write data mask (DM) pin for each data byte (DQ) is supported, consistent with the implementation on LPDDR3 SDRAM. Each DM can mask its respective DQ for any given cycle of the burst. Data mask timings match data bit timing, but are inputs only. Internal data-mask loading is identical to data-bit loading to ensure matched system timing.

Figure. Data Mask Timing





Note.
1. For the data mask function, BL=8 is shown; the second data bit is masked.

Precharge

The PRECHARGE command is used to precharge or close a bank that has been activated. The PRECHARGE command is initiated with CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The PRECHARGE command can be used to precharge each bank independently or all banks simultaneously. The AB flag and the bank address bits BA0, BA1, and BA2 are used to determine which bank(s) to precharge. The precharged bank(s) will be available for subsequent row access tRPab after an all-bank PRECHARGE command is issued, or tRPpb after a single-bank PRECHARGE command is issued.

To ensure that LPDDR3 devices can meet the instantaneous current demand required to operate, the row-precharge time for an all-bank PRECHARGE (tRPab) will be longer than the row PRECHARGE time for a single-bank PRECHARGE (tRPpb).

Table. Bank selection for Precharge by address bits

AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s) 8-bank device
0	0	0	0	Bank 0 only
0	0	0	1	Bank 1 only
0	0	1	0	Bank 2 only
0	0	1	1	Bank 3 only
0	1	0	0	Bank 4 only
0	1	0	1	Bank 5 only
0	1	1	0	Bank 6 only
0	1	1	1	Bank 7 only
1	Don’t Care	Don’t Care	Don’t Care	All Banks

Burst read operation followed by Precharge

For the earliest possible precharge, the PRECHARGE command can be issued BL/2 clock cycles after a READ command. A new bank ACTIVATE command can be issued to the same bank after the row PRECHARGE time (tRP) has elapsed. A PRECHARGE command cannot be issued until after tRAS is satisfied. The minimum READ-to-PRECHARGE time must also satisfy a minimum analog time from the rising clock edge that initiates the last 8-bit prefetch of a READ command. tRTP begins BL/2 - 4 clock cycles after the READ command. (optional) If the burst is truncated by a BST command or a Read command to a different bank, the effective "BL" shall be used to calculate when tRTP begins.

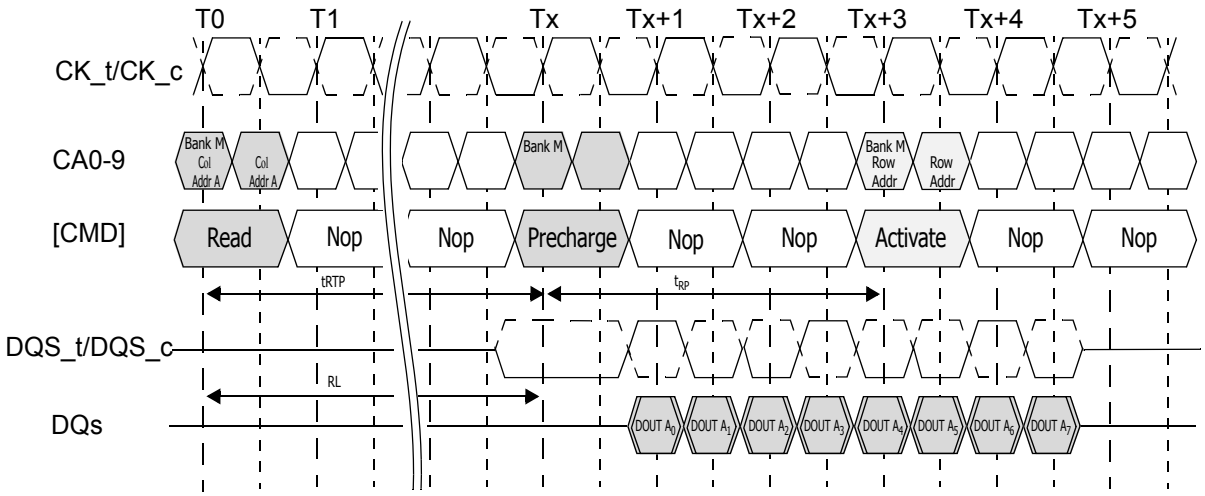


Figure. Burst read followed by Precharge

Burst write followed by precharge

For WRITE cycles, a WRITE recovery time (tWR) must be provided before a PRECHARGE command can be issued. This delay is referenced from the last valid burst input data to the completion of the burst WRITE. PRECHARGE command must not be issued prior to the tWR delay.

LPDDR3 devices write data to the array in prefetch multiples(prefetch = 8). An internal WRITE operation can only begin after a prefetch group has been completely latched, so tWR starts at prefetch boundaries. The minimum WRITE-to-PRECHARGE time for commands to the same bank is WL + BL/2 + 1 + RU(tWR/tCK) clock cycles. (optional) For an untruncated burst, BL is the value from the Mode Register. For an truncated burst, BL is the effective burst length.

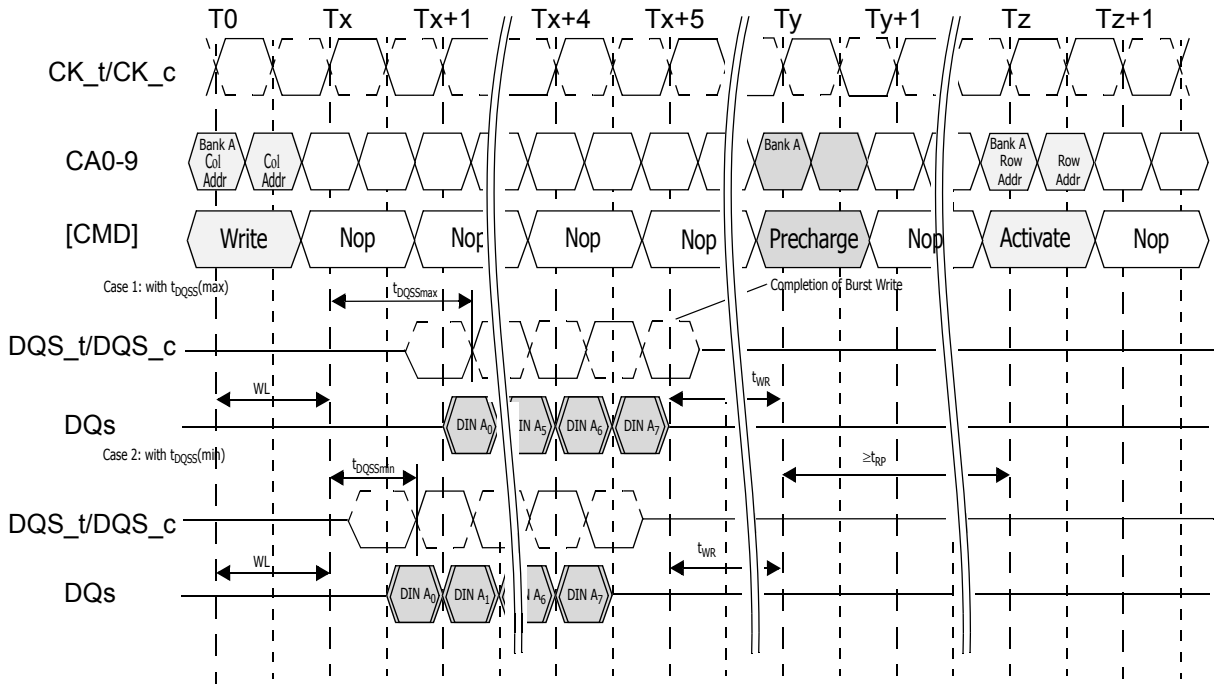


Figure. Burst write followed by Precharge

Auto Precharge Operation

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the auto precharge function. When a READ or a WRITE command is issued to the device, the AP bit (CA0f) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ or WRITE cycle.

If AP is LOW when the READ or WRITE command is issued, then normal READ or WRITE burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the READ or WRITE command is issued, the auto precharge function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency) thus improving system performance for random data access.

Burst Read with Auto Precharge

If AP (CA0f) is HIGH when a READ command is issued, the READ with auto-precharge function is engaged. LPDDR3 devices start an auto-precharge operation on the rising edge of the clock BL/2 or BL/2 - 2 4+ RU(tRTP/tCK) clock cycles later than the READ with auto precharge command, whichever is greater. For LPDDR3 auto-precharge calculations see the table in the next page. Following an auto-precharge operation, an ACTIVATE command can be issued to the same bank if the following two conditions are satisfied simultaneously:

a) The RAS precharge time (tRP) has been satisfied from the clock at which the auto- precharge begins.

b) The RAS cycle time (tRC) from the previous bank activation has been satisfied.

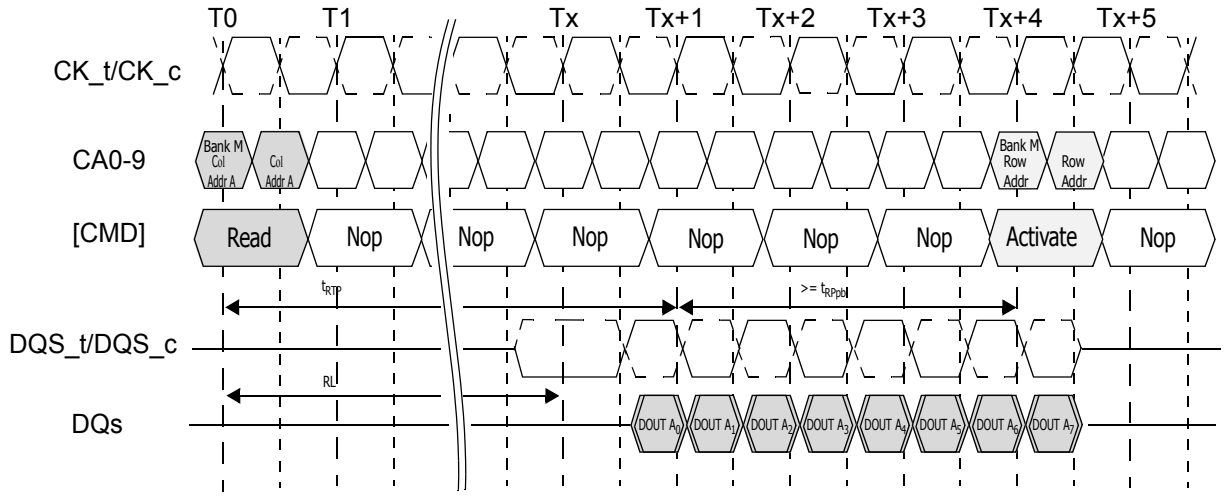


Figure. Burst read with Auto-Precharge

Burst Write with Auto Precharge

If AP (CA0f) is HIGH when a WRITE command is issued, the WRITE with auto precharge function is engaged. The device starts an auto precharge on the rising edge tWR cycles after the completion of the burst WRITE. Following a WRITE with auto precharge, an ACTIVATE command can be issued to the same bank if the following two conditions are met:

The RAS precharge time (tRP) has been satisfied from the clock at which the auto- precharge begins.

The RAS cycle time (tRC) from the previous bank activation has been satisfied.

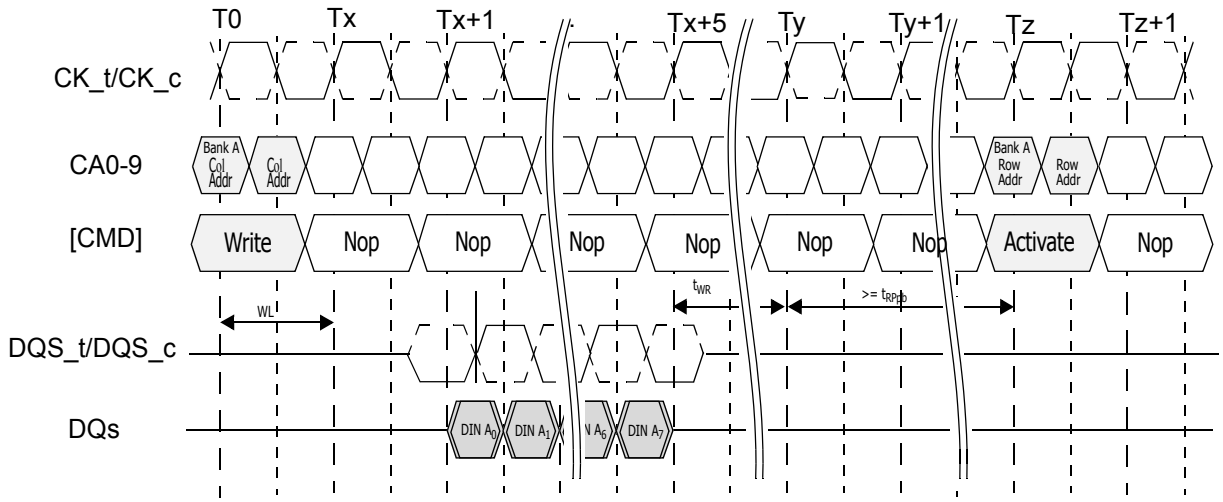


Figure. Burst write with Auto Precharge

Table. Precharge and auto precharge clarification

From command	To command	Minimum delay between From command to To command	Unit	Notes
Read	Precharge (to same bank as read)	BL/2 + max(4, RU (tRTP/tCK)) - 4	CLK	1
	Precharge All	BL/2 + max(4, RU (tRTP/tCK)) - 4	CLK	1
BST (for Reads)	Precharge (to same bank as read)	1	CLK	1
	Precharge All	1	CLK	1
Read w/ AP	Precharge (to same bank as read w/ AP)	BL/2 + max(4, RU (tRTP/tCK)) - 4	CLK	1
	Precharge All	BL/2 + max(4, RU (tRTP/tCK)) - 4	CLK	1
	Activate (to same bank as read w/ AP)	BL/2 + max(4, RU (tRTP/tCK)) - 4 + RU(tRPpb/tCK)	CLK	1
	Write or Write w/AP (same bank)	Illegal	CLK	3
	Write or Write w/AP (different bank)	RL + BL/2 + RU(tDQSCKmax/tCK) -WL + 1	CLK	3
	Read or Read w/AP (same bank)	Illegal	CLK	3
	Read or Read w/AP (different bank)	BL/2	CLK	3
Write	Precharge (to same bank as write)	WL + BL/2 + RU (tWR/tCK) + 1	CLK	1
	Precharge All	WL + BL/2 + RU (tWR/tCK) + 1	CLK	1
BST (for Writes)	Precharge (to same bank as Write)	WL + RU(tWR/tCK) + 1	CLK	1
	Precharge All	WL + RU(tWR/tCK) + 1	CLK	1
Write w/ AP	Precharge (to same bank as write w/ AP)	WL + BL/2 + RU (tWR/tCK) + 1	CLK	1
	Precharge All	WL + BL/2 + RU (tWR/tCK) + 1	CLK	1
	Activate (to same bank as write w/ AP)	WL + BL/2 + RU (tWR/tCK) + 1 + RU(tRPpb/tCK)	CLK	1
	Write or Write w/AP (same bank)	Illegal	CLK	3
	Write or Write w/AP (different bank)	BL/2	CLK	3
	Read or Read w/AP (same bank)	Illegal	CLK	3
	Read or Read w/AP (different bank)	WL + BL/2 + RU(tWTR/tCK) + 1	CLK	3
Precharge	Precharge (to same bank as precharge)	1	CLK	1
	Precharge All	1	CLK	1
Precharge All	Precharge	1	CLK	1
	Precharge All	1	CLK	1

Note:

1. For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after tRP depending on the latest precharge command issued to that bank.
2. Any command issued during the minimum delay time as specified in Table above is illegal.
3. After Read with AP, seamless read operations to different banks are supported. After Write with AP, seamless write operations to different banks are supported. Read w/AP and Write w/AP may not be interrupted or truncated.

Refresh Command

The REFRESH command is initiated with CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. Per-bank REFRESH is initiated with CA3 LOW at the rising edge of the clock. All-bank REFRESH is initiated with CA3 HIGH at the rising edge of the clock.

A per-bank REFRESH command (REFpb) performs a per-bank REFRESH operation to the bank scheduled by the bank counter in the memory device. The bank sequence for per-bank REFRESH is fixed to be a sequential round-robin: 0-1-2-3-4-5-6-7-0-1-.... The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon issuing a RESET command or at every exit from self refresh. Bank addressing for the per-bank REFRESH count is the same as established for the single-bank PRECHARGE command. A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions are met:

- tRFCab has been satisfied after the prior REFab command
- tRFCpb has been satisfied after the prior REFpb command
- tRP has been satisfied after the prior Precharge command to that given bank

tRRD has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than the one affected by the REFpb command).

The target bank is inaccessible during per-bank REFRESH cycle time (tRFCpb), however, other banks within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or a WRITE command. When the per-bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, these conditions must be met:

- tRFCpb must be satisfied before issuing a REFab command
- tRFCpb must be satisfied before issuing an ACTIVATE command to the same bank
- tRRD must be satisfied before issuing an ACTIVATE command to a different bank
- tRFCpb must be satisfied before issuing another REFpb command

An all-bank REFRESH command (REFab) issues a REFRESH command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE-all command prior to issuing an all-bank REFRESH command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met:

- tRFCab has been satisfied after the prior REFab command
- tRFCpb has been satisfied after the prior REFpb command
- tRP has been satisfied after prior Precharge commands

When an all-bank refresh cycle has completed, all banks will be idle. After issuing REFab:

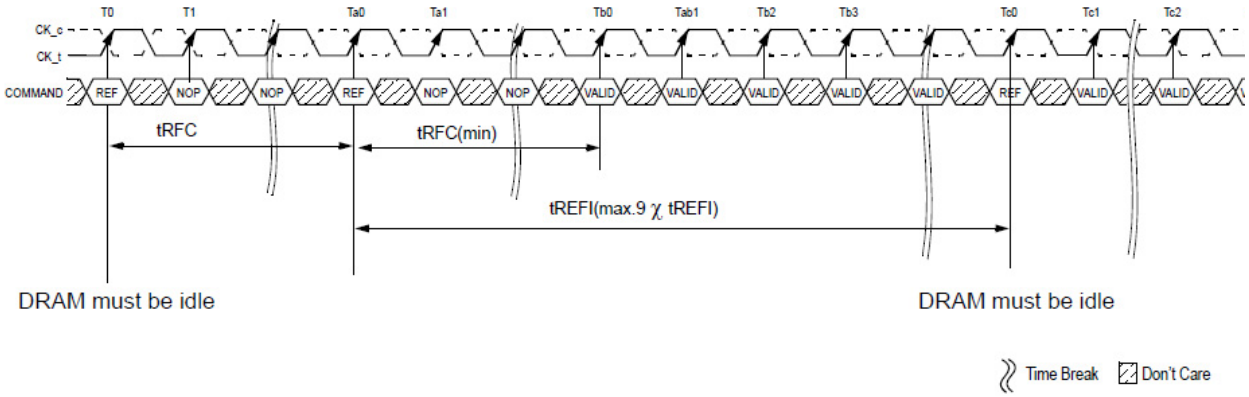
- tRFCab latency must be satisfied before issuing an ACTIVATE command
- tRFCab latency must be satisfied before issuing a REFab or REFpb command

Table. Command Scheduling Separations related to Refresh

Symbol	minimum delay from	to	Notes
tRFCab	REFab	REFab	
		Activate command to any bank	
		REFpb	
tRFCpb	REFpb	REFab	
		Activate command to same bank as REFpb	
		REFpb	
tRRD	REFpb	Activate command to different bank than REFpb	
	Activate	REFpb	1
		Activate command to different bank than prior Activate command	

Note:
1. A bank must be in the idle state before it is refreshed, so following an ACTIVATE command REFab is prohibited; REFpb is supported only if it affects a bank that is in the idle state.

In general, an all bank refresh command needs to be issued to the LPDDR3 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided for postponing and pulling-in refresh command. A maximum of 8 Refresh commands can be postponed during operation of the LPDDR3 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 × tREFI (see Figure 1). A maximum of 8 additional Refresh commands can be issued in advance ("pulled in") , with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8, depending on Refresh mode, Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 9 × tREFI . At any given time, a maximum of 16 REF commands can be issued within 2 x tREFI.
And for per bank refresh, a maximum 8 x 8 per bank refresh commands can be postponed or pulled in for scheduling efficiency. At any given time, a maximum of 2 x 8 x 8 per bank refresh commands can be issued within 2 x tREFI.



Note.
1. Only NOP commands allowed after Refresh command registered untill tRFC(min) expires.
2. Time interval between two Refresh commands may be extended to a maximum of 9 X tREFI.

Figure. Refresh Command Timing

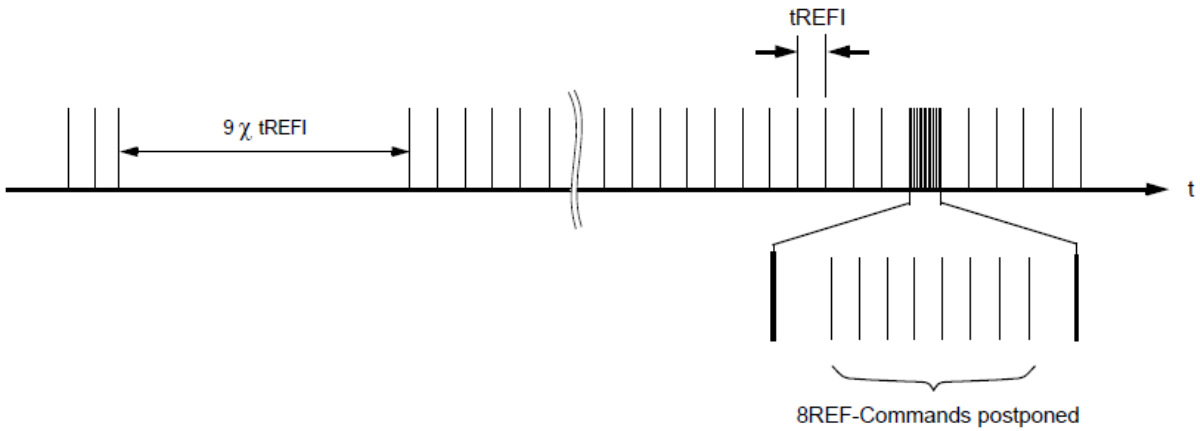


Figure. Postponing Refresh Commands

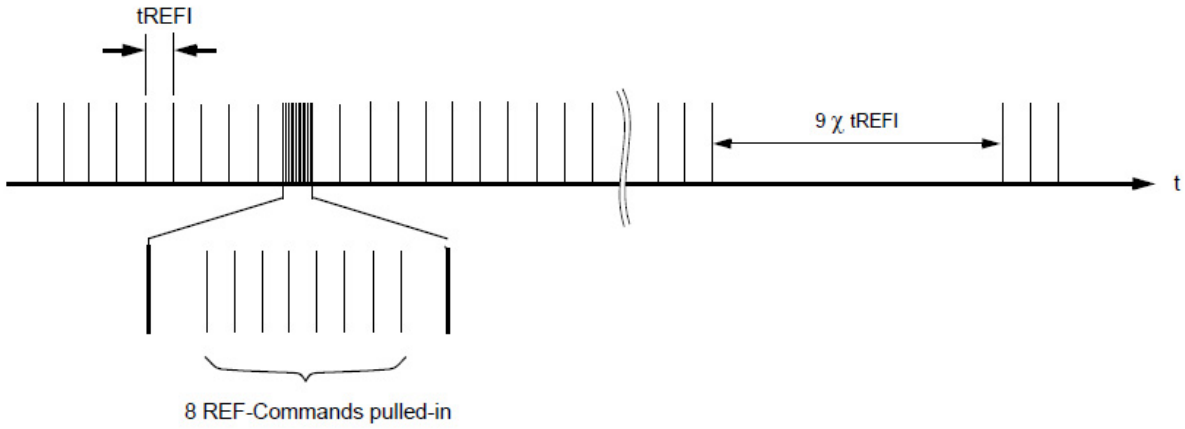


Figure. Pulling-in Refresh Commands

Refresh Requirements

1.Minimum number of REFRESH commands

LPDDR3 requires a minimum number, R, of REFRESH (REFab) commands within any rolling refresh window (tREFW = 32 ms @ MR4[2:0] = 011 or TC ≤ 85°C). For tREFW and tREFI refresh multipliers at different MR4 settings, refer to the MR4 definition.

When using per-bank REFRESH, a REFab command can be replaced by a full cycle of eight REFpb commands.

2.Burst REFRESH limitation

Self refresh mode may be entered with a maximum of eight refresh commands being postponed. After exiting self-refresh mode with one or more refresh commands postponed, additional refresh commands may be postponed to the extent that the total number of postponed refresh commands (before and after the self refresh) will never exceed eight. During self-refresh mode, the number of postponed or pulled-in REF commands does not change.

The use of self refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from self refresh mode. Upon exit from self refresh, the LPDDR3 SDRAM requires a minimum of one extra refresh command before it is put back into self refresh mode.

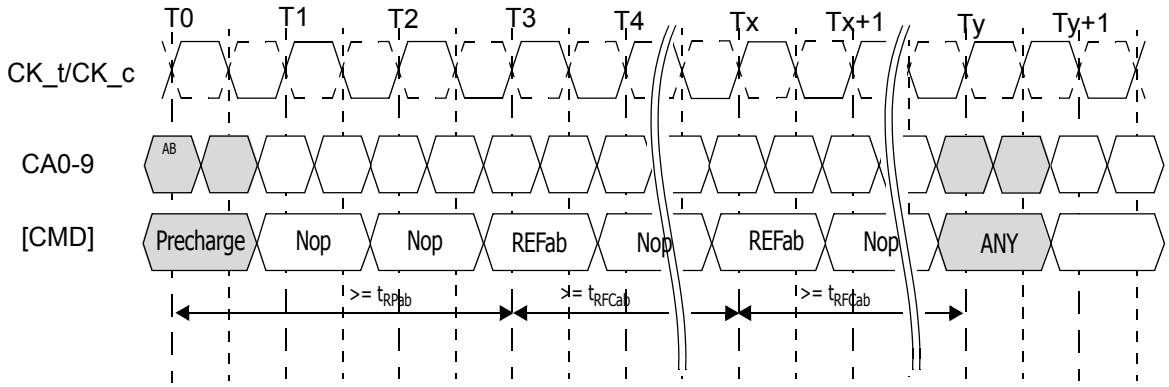
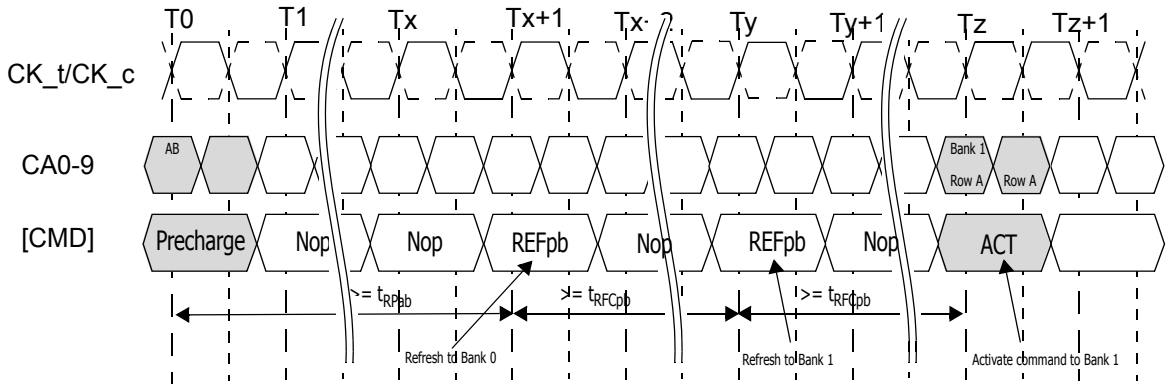


Figure. All Bank Refresh Operation



Note:

1. In the beginning of this example, the REFpb bank is pointing to Bank 0.
2. Operations to other banks than the bank being refreshed are allowed during the t_{RFCpb} period.

Figure. Per Bank Refresh Operation

Self refresh operation

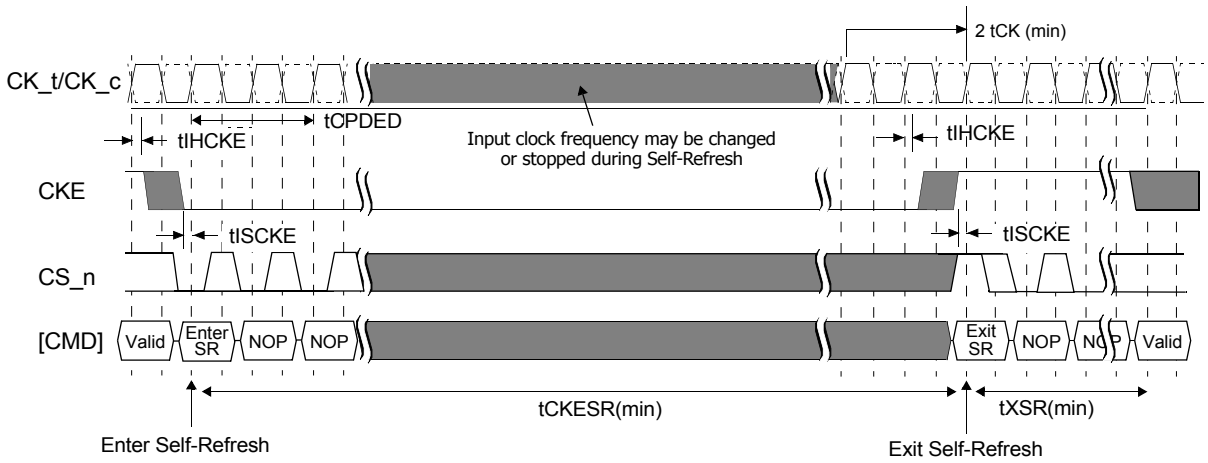
The Self Refresh command can be used to retain data in the LPDDR3 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the SDRAM retains data without external clocking. The device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having CKE LOW, CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the previous clock cycle. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW, this timing period is defined as tCPDED. CKE LOW will result in deactivation of input receivers after tCPDED has expired. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode.

LPDDR3 SDRAM devices can operate in Self Refresh in both the standard or elevated temperature ranges. LPDDR3 devices will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperatures and higher at high temperatures.

Once the SDRAM has entered Self Refresh mode, all of the external signals except CKE, are "don't care". For proper self refresh operation, power supply pins (VDD1, VDD2, and VDDCA) must be at valid levels. VDDQ may be turned off during Self-Refresh. Prior to exiting Self-Refresh, VDDQ must be within specified limits. VrefDQ and VrefCA may be at any level within minimum and maximum levels (see Absolute Maximum DC Ratings). However prior to exiting Self-Refresh, VrefDQ and VrefCA must be within specified limits (see Recommended DC Operating Conditions). The SDRAM initiates a minimum of one all-bank refresh command internally within tCKESR period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the SDRAM must remain in Self Refresh mode is tCKESR. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock shall be stable and within specified limits for a minimum of 2 tCK prior to the positive clock edge that registers CKE HIGH. Once Self Refresh Exit is registered, a delay of at least tXSR must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period tXSR for proper operation except for self refresh re-entry. NOP commands must be registered on each positive clock edge during the Self Refresh exit interval tXSR.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, it is required that at least one Refresh command (8 per-bank or 1 all-bank) is issued before entry into a subsequent Self Refresh.



Note:

1. Input clock frequency may be changed or stopped during self-refresh, provided that upon exiting self-refresh, a minimum of 2 clocks of stable clock are provided and the clock frequency is between the minimum and maximum frequency for the particular speed grade.
2. Device must be in the "All banks idle" state prior to entering Self Refresh mode.
3. tXSR begins at the rising edge of the clock after CKE is driven HIGH.
4. A valid command may be issued only after tXSR is satisfied. NOPs shall be issued during tXSR.

Figure. Self Refresh Operation

Partial Array Self Refresh: Bank Masking

LPDDR3 SDRAM has 8 banks (additional banks may be required for higher densities). Each bank of LPDDR3 SDRAM can be independently configured whether a self refresh operation is taking place. One mode register unit of 8 bits accessible via MRW command is assigned to program the bank masking status of each bank up to 8 banks. For bank masking bit assignments see Mode Register 16.

The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to the entire bank is blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, a coupled mask bit has to be programmed, "unmasked". When a bank mask bit is unmasked, a refresh to a bank is determined by the programmed status of segment mask bits, which is described in the following chapter.

Partial Array Self Refresh: Segment Masking

Segment masking scheme may be used in lieu of or in combination with bank masking scheme in LPDDR3 SDRAM. LPDDR3 devices utilize 8 segments per bank. For segment masking bit assignments, see Mode Register 17.

For those refresh-enabled banks, a refresh operation to the address range which is represented by a segment is blocked when the mask bit to this segment is programmed, "masked". Programming of segment mask bits is similar to the one of bank mask bits. With LPDDR3, 8 segments are used as listed in Mode Register 17. One mode register unit is used for the programming of segment mask bits up to 8 bits. One more mode register unit may be reserved for future use. Programming of bits in the reserved registers has no effect on the device operation.

Table: Example of Bank and Segment Masking use in LPDDR3 devices

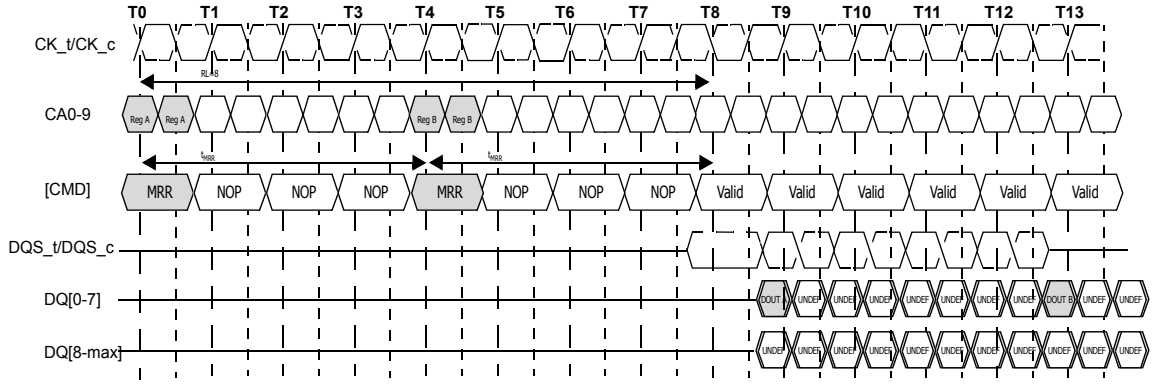
	Segment Mask (MR17)	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
Bank Mask (MR16)		**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**
Segment 0	**0**		**M**						**M**
Segment 1	**0**		**M**						**M**
Segment 2	**1**	**M**	**M**	**M**	**M**	**M**	**M**	**M**	**M**
Segment 3	**0**		**M**						**M**
Segment 4	**0**		**M**						**M**
Segment 5	**0**		**M**						**M**
Segment 6	**0**		**M**						**M**
Segment 7	**1**	**M**	**M**	**M**	**M**	**M**	**M**	**M**	**M**

Note: 1. This table illustrates an example of an 8-bank LPDDR3 device, when a refresh operation to bank 1 and bank 7, as well as segment 2 and segment 7 are masked.

Mode Register Read Command

The MRR command is used to read configuration and status data from SDRAM mode registers. The MRR command is initiated with CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by CA1f–CA0f and CA9r–CA4r. The mode register contents are available on the first data beat of DQ[7:0] after RL × tCK + tDQSCK + tDQSQ following the rising edge of the clock where MRR is issued. Subsequent data beats contain valid but undefined content, except in the case of the DQ calibration function, where subsequent data beats contain valid content as described in the DQ Calibration specification. All DQS are toggled for the duration of the mode register READ burst.

The MRR command has a burst length of eight. MRR operation (consisting of the MRR command and the corresponding data traffic) must not be interrupted.

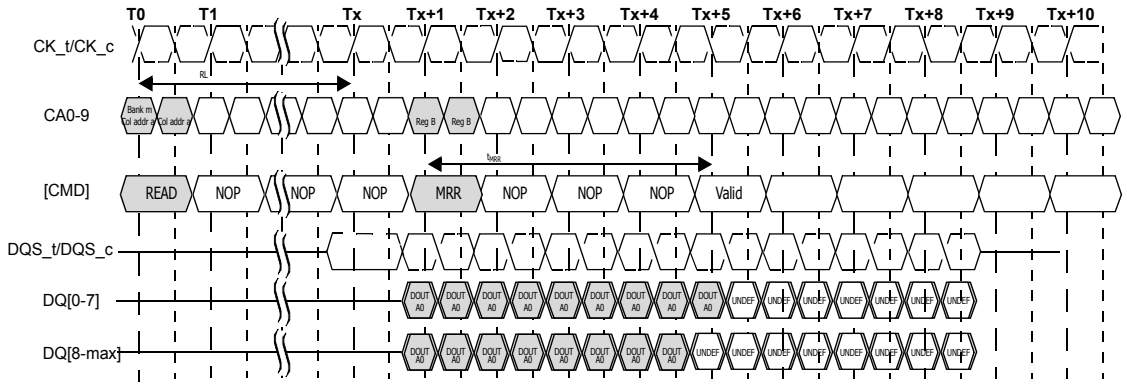


Note:

1. MRRs to DQ calibration registers MR32 and MR40 are described in DQ calibration section.
2. Only the NOP command is supported during tMRR.
3. Mode register data is valid only on DQ[7:0] on the first beat. Subsequent beats contain valid but undefined data. DQ[MAX:8] contain valid but undefined data for the duration of the MRR burst.
4. Minimum Mode Register Read to write latency is RL + RU(tDQSCKmax/tCK) + 8/2 + 1 - WL clock cycles.
5. Minimum Mode Register Read to Mode Register Write latency is RL + RU(tDQSCKmax/tCK) + 8/2 + 1clock cycles.
6. In this example, RL = 8 for illustration purposes only.

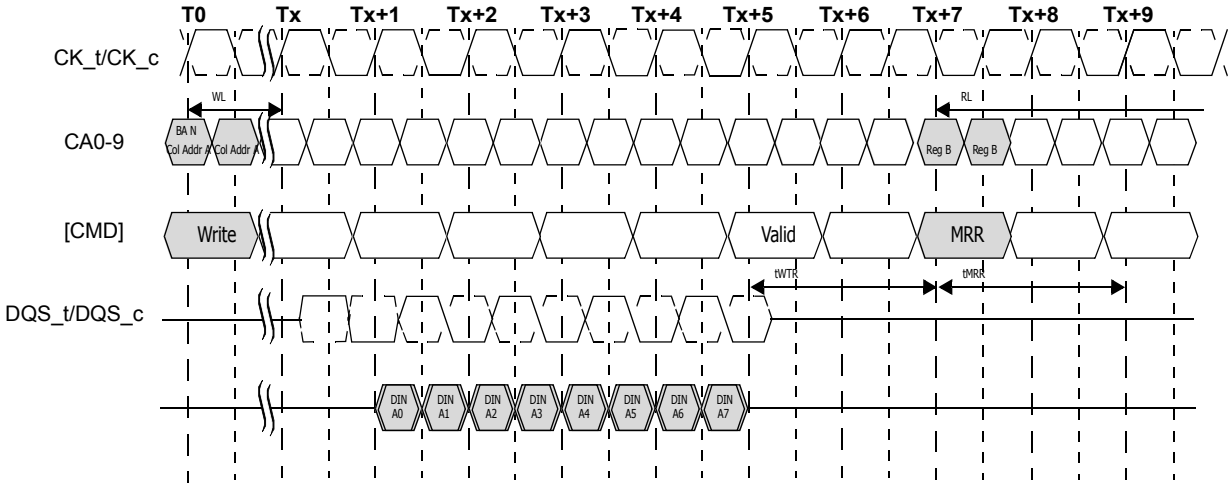
Figure. Mode Register Read Timing

After a prior READ command, the MRR command must not be issued earlier than BL/2 clock cycles, or WL + 1 + BL/2 + RU(tWTR/tCK) clock cycles after a prior WRITE command, as READ bursts and WRITE bursts must not be truncated by MRR.



Note:
1.Only the NOP command is supported during tMRR.
2.The minimum number of clock cycles from the burst READ command to the MRR command is BL/2.

Figure. Read to MRR timing

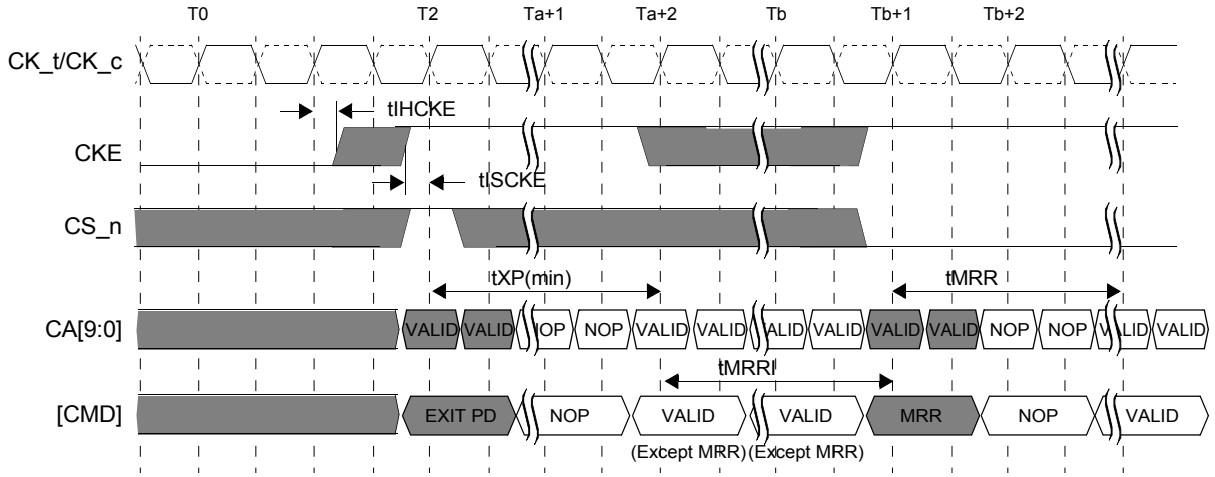


Note:
1.The minimum number of clock cycles from the burst WRITE command to the MRR command is [WL + 1 + BL/2 + RU(tWTR/tCK)].
2. Only the NOP command is supported during tMRR.

Figure. Burst Write Followed by MRR

MRR Following Idle Power-Down State

Following the idle power-down state, an additional time, tMRRI, is required prior to issuing the mode register read (MRR) command. This additional time (equivalent to tRCD) is required in order to be able to maximize power-down current savings by allowing more power-up time for the MRR data path after exit from standby, idle power-down mode.



Note:

1. Any valid command from the idle state except MRR.
2. tMRRI = tRCD.

Figure. MRR Following Power-Down Idle State

Temperature Sensor

LPDDR3 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing de-rating is required in the elevated temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device TOPER (See Operating Temperature Range) may be used to determine whether operating temperature requirements are being met.

LPDDR3 devices shall monitor device temperature and update MR4 according to tTSI. Upon exiting self-refresh or power-down, the device temperature status bits shall be no older than tTSI.

When using the temperature sensor, the actual device case temperature may be higher than the TOPER specification (See Operating Temperature Range) that applies for the standard or elevated temperature ranges. For example, TCASE may be above 85°C when MR4[2:0] equals 011B. LPDDR3 devices shall allow for a 2°C temperature margin between the point at which the device temperature enters the elevated temperature range and point at which the controller re-configures the system accordingly. In the case of tight thermal coupling of the memory device to external hot spots, the maximum device temperature might be higher than what is indicated by MR4.

To assure proper operation using the temperature sensor, applications should consider the following factors:
- TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2'C.
- ReadInterval is the time period between MR4 reads from the system.
- TempSensorInterval (tTSI) is maximum delay between internal updates of MR4.
- SysRespDelay is the maximum time between a read of MR4 and the response by the system.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$\textit{TempGradient x (ReadInterval + tTSI + SysRespDelay)} \leq \textit{2}^{o}\textit{C}$$

Paramter	Sysmbol	Min/Max	Value	Unit	Note
System Temperature Gradient	TempGradient	Max	System Dependent	^{o}C/s	
MR4 Read Interval	ReadInterval	Max	System Dependent	ms	
Temperature Sensor Interval	tTSI	Max	32	ms	
System Response Delay	SysRespDelay	Max	System Dependent	ms	
MR4 Temp Margin	TempMargin	Max	2	^{o}C	

For example, if TempGradient is 10^{o}C/s and the SysRespDelay is 1ms:

$$10^{o}C/s \times (ReadInterval + 32ms + 1ms) <= 2^{o}C$$

In this case, ReadInterval shall be no greater than 167ms.

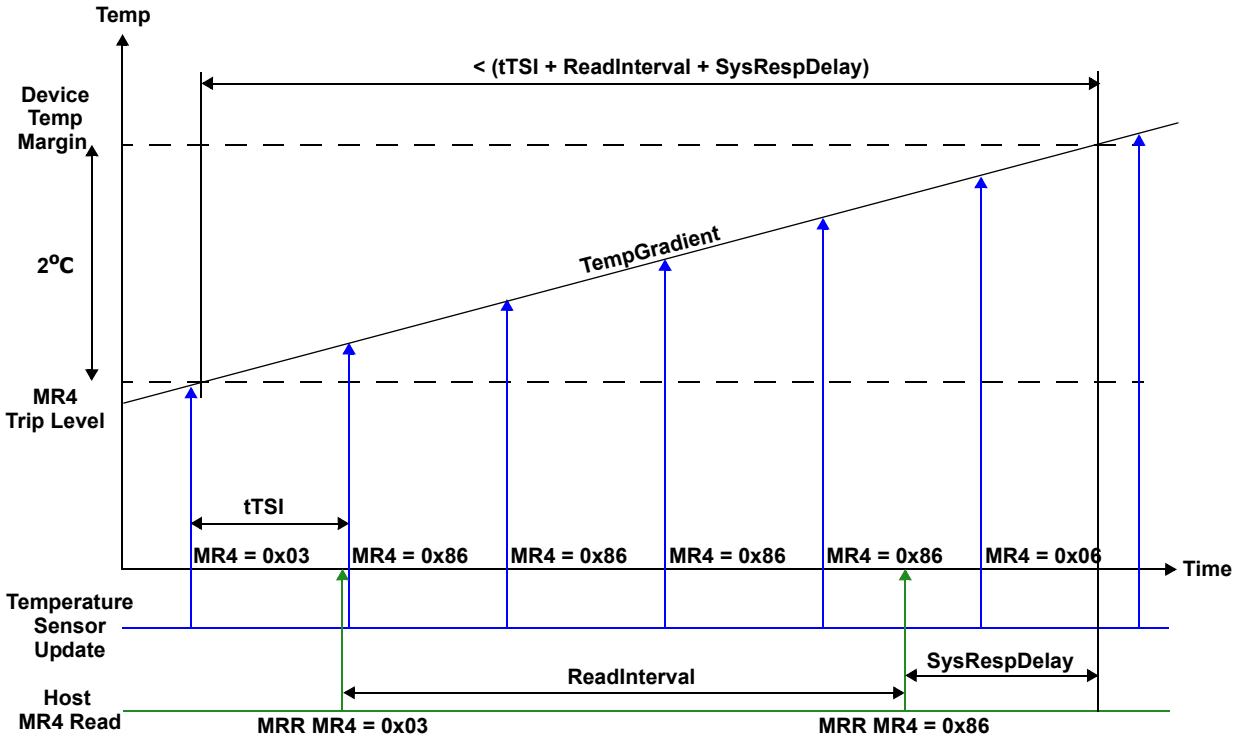


Figure. Temp Sensor Timing

DQ Calibration

LPDDR3 device features a DQ calibration function that outputs one of two predefined system timng calibration patterns. A Mode Register Read to MR32 (Pattern "A") or MR40 (Pattern "B") will return the specified pattern on DQ[0] and DQ[8] for X16 devices, and DQ[0], DQ[8], DQ[16], and DQ[24] for X32 devices. For X16 devices, DQ[7:1] and DQ[15:9] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst. For X32 devices, DQ[7:1], DQ[15:9], DQ[23:17],and DQ[31:25] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst.

Table. Data Calibration Pattern Description

	Bit Time 0	Bit Time 1	Bit TIme 2	Bit Time 3	Bit Time 4	Bit Time 5	Bit Time 6	Bit Time 7
Pattern A (MR32)	1	0	1	0	1	0	1	0
Pattern B (MR40)	0	0	1	1	0	0	1	1

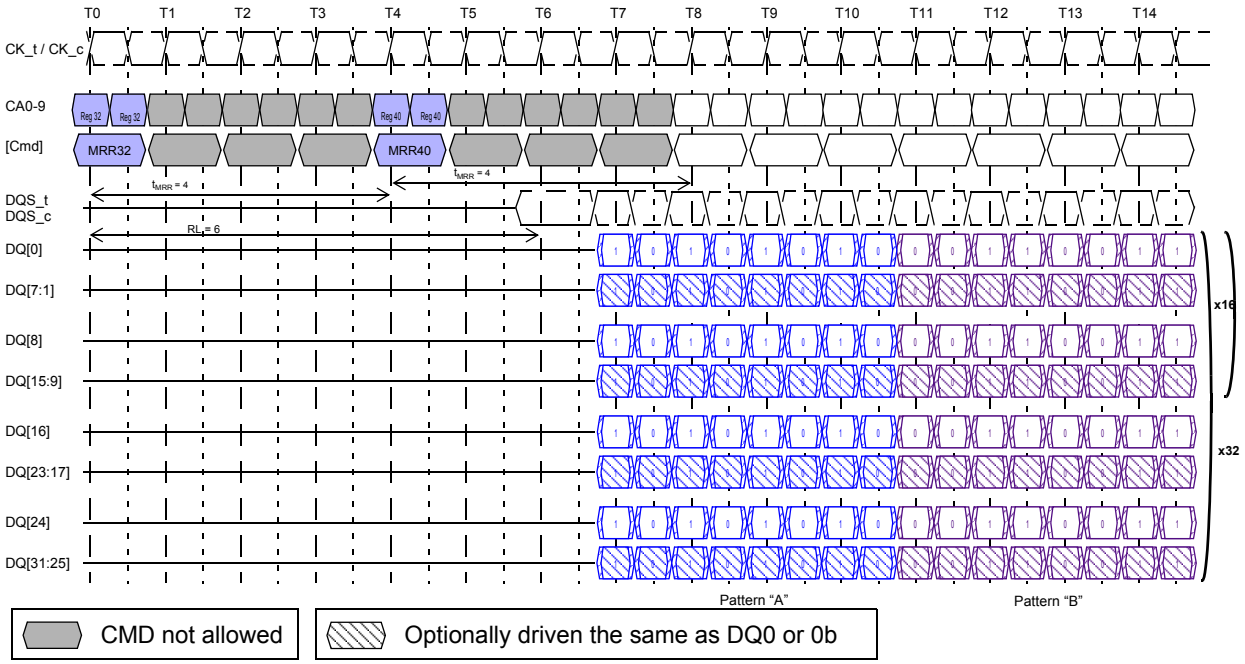
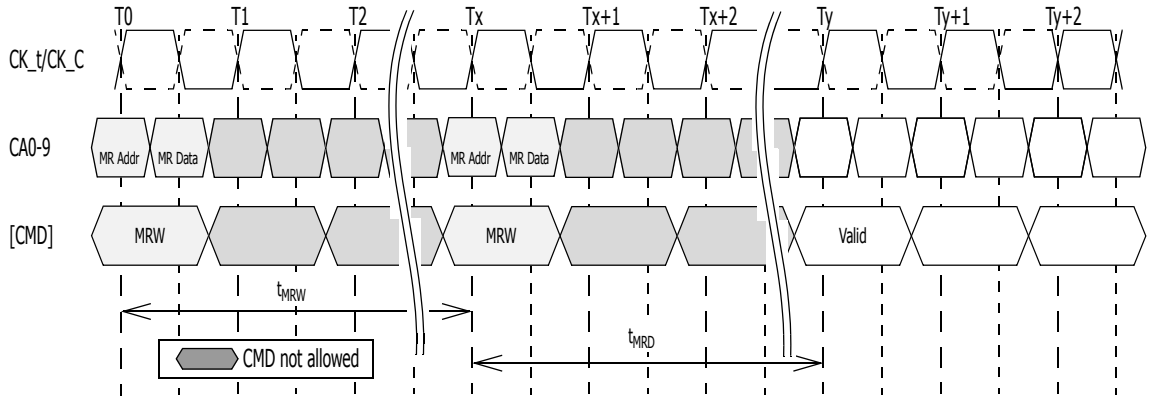


Figure. MR32 and MR40 DQ Calibration timing example

Note:
1. Mode Register Read has a burst length of eight.
2. Mode Register Read operation shall not be interrupted.
3. Mode Register Reads to MR32 and MR40 drive valid data on DQ[0] during the entire burst. For X16 devices, DQ[8] shall drive the same information as DQ[0] during the burst. For X32 devices, DQ[8], DQ[16] and DQ[24] shall drive the same information as DQ[0] during the burst.
4. For X16 devices, DQ[7:1] and DQ[15:9] may optionally drive the same information as DQ[0] or they may drive 0b during the burst. For X32 devices, DQ[7:1], DQ[15:9], DQ[23:17] and DQ[31:25] may optionally drive the same information as DQ[0] or they may drive 0b during the burst.

Mode Register Write Command

The MRW command is used to write configuration data to mode registers. The MRW command is initiated with CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by CA1f-CA0f, CA9r-CA4r. The data to be written to the mode register is contained in CA9f-CA2f. The MRW command period is defined by tMRW. Mode register WRITEs to read-only registers have no impact on the functionality of the device.



Note:

1. At time Ty, the device is in the idle state.
2. Only the NOP command is supported during tMRW.

Figure. Mode Register Write timing example

Mode Register Write

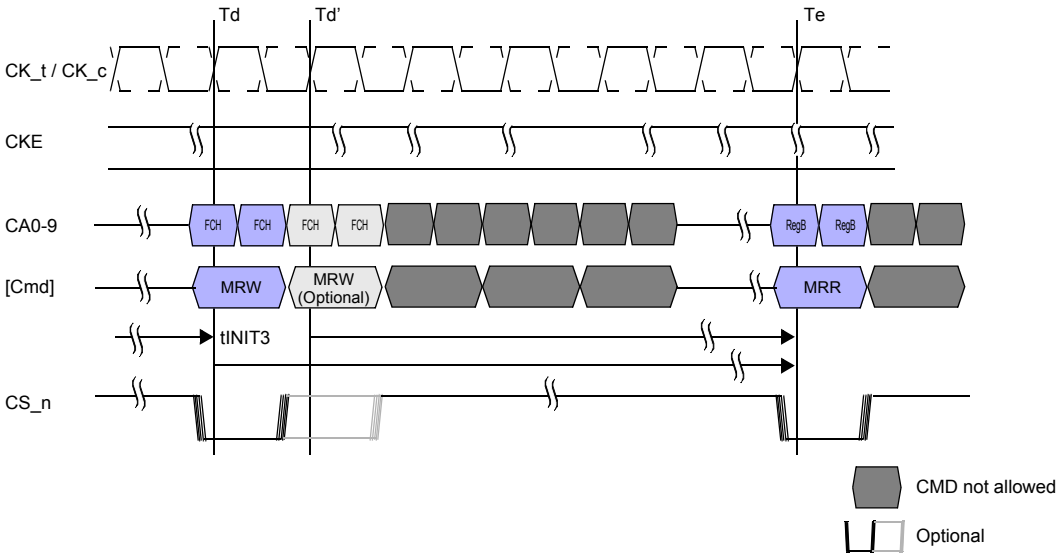
MRW can only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in this state is to issue a PRECHARGE-ALL command.

MRW Reset

The MRW RESET command brings the device to the device auto-initialization (resetting) state in the power-on initialization sequence. The MRW RESET command can be issued from the idle state. This command resets all mode registers to their default values. After MRW RESET, boot timings must be observed until the device initialization sequence is complete and the device is in the idle state. Array data is undefined after the MRW RESET command.

If the initialization is to be performed at-speed (greater than the recommended boot clock frequency), then CA Training may be necessary to ensure setup and hold timings. Since the MRW RESET command is required prior to CA Training an alternate MRW RESET command with an op-code of 0xFCh should be used. This encoding ensures that no transitions occur on the CA bus. Prior to CA Training, it is recommended to hold the CA bus stable for one cycle prior to, and one cycle after, the issuance of the MRW RESET command to ensure setup and hold timings on the CA bus.

Current State	Command	Intermediate State	Next State
All Banks Idle	MRR	Mode Register Reading (All Banks Idle)	All Banks Idle
	MRW	Mode Register Writing (All Banks Idle)	All Banks Idle
	MRW (RESET)	Resetting (Device Auto-Init)	All Banks Idle
Bank(s) Active	MRR	Mode Register Reading (Bank(s) Active)	Bank(s) Active
	MRW	Not Allowed	Not Allowed
	MRW (RESET)	Not Allowed	Not Allowed



Note:
1. Optional MRW RESET command and optional CS_n assertion are allowed, When optional MRW RESET command is used, tINIT4 starts at Td'.

Figure. Mode Register Write Timing for MRW RESET

Mode Register Write ZQ Calibration Command

The MRW command is used to initiate the ZQ calibration command. This command is used to calibrate the output driver impedance across process, temperature, and voltage. LPDDR3 devices support ZQ calibration.

There are four ZQ calibration commands and related timings: tZQINIT, tZQRESET, tZQCL, and tZQCS. tZQINIT is for initialization calibration; tZQRESET is for resetting ZQ to the default output impedance; tZQCL is for long calibration(s); and tZQCS is for short calibration(s).

The initialization ZQ calibration (ZQINIT) must be performed for LPDDR3. ZQINIT provides an output impedance accuracy of ±15 percent. After initialization, the ZQ calibration long (ZQCL) can be used to recalibrate the system to an output impedance accuracy of ±15 percent. A ZQ calibration short (ZQCS) can be used periodically to compensate for temperature and voltage drift in the system.

The ZQ reset command (ZQRESET) resets the output impedance calibration to a default accuracy of ±30% across process, voltage, and temperature. This command is used to ensure output impedance accuracy to ±30% when ZQCS and ZQCL commands are not used.

One ZQCS command can effectively correct at least 1.5% (ZQ correction) of output impedance errors within tZQCS for all speed bins, assuming the maximum sensitivities specified are met. The appropriate interval between ZQCS commands can be determined from using these tables and system-specific parameters.

LPDDR3 devices are subject to temperature drift rate (TdriftrateE) and voltage drift rate (Vdriftrate) in various applications. To accommodate drift rates and calculate the necessary interval between ZQCS commands, apply the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

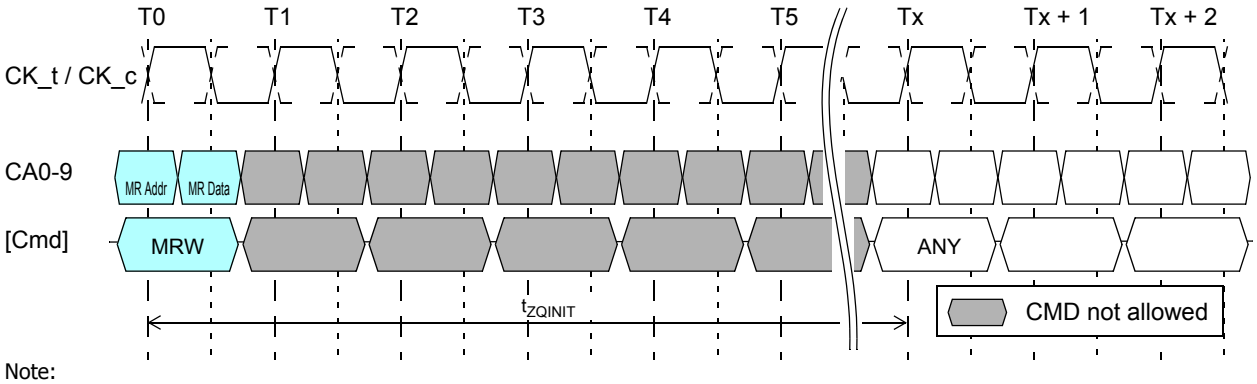
where TSens = max(dRONdT) and VSens = max(dRONdV) define the LPDDR3 temperature and voltage sensitivities.

For example, if TSens = 0.75% / °C, VSens = 0.20% / mV, Tdriftrate = 1°C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$

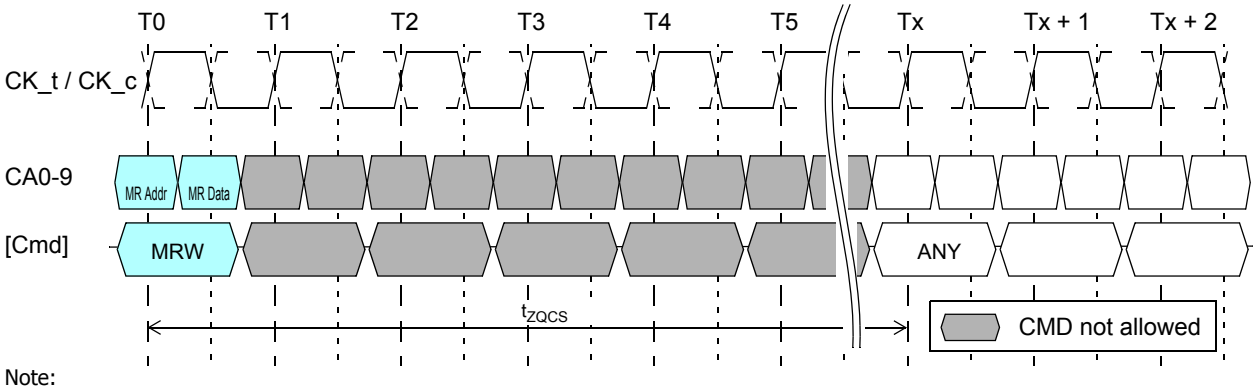
A ZQ calibration command can only be issued when the device is in the idle state with all banks precharged.

No other activities can be performed on the data bus during calibration periods (tZQINIT, tZQCL, or tZQCS). The quiet time on the data bus helps to accurately calibrate output impedance. There is no required quiet time after the ZQ RESET command. If multiple devices share a single ZQ resistor, only one device can be calibrating at any given time. After calibration is complete, the ZQ ball circuitry is disabled to reduce power consumption. In systems sharing a ZQ resistor between devices, the controller must prevent tZQINIT, tZQCS, and tZQCL overlap between the devices. ZQ RESET overlap is acceptable.



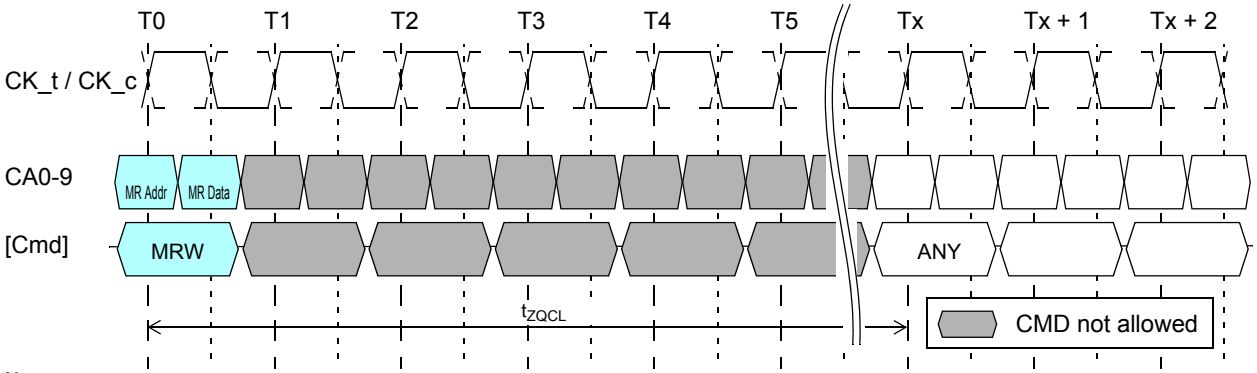
Note:
1. Only the NOP command is supported during ZQ calibration.
2. CKE must be registered HIGH continuously during the calibration period.
3. All devices connected to the DQ bus should be High-Z during the calibration process

Figure. ZQ Calibration Initialization timing



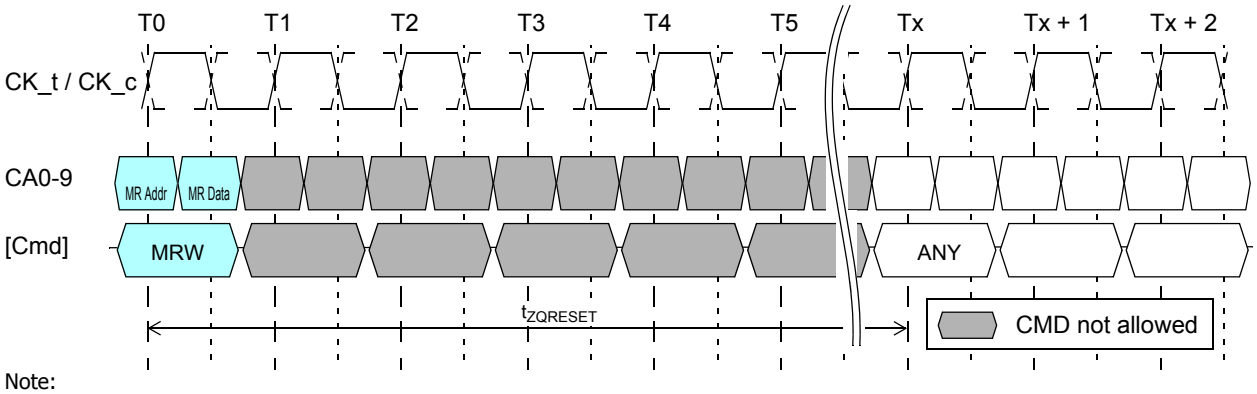
Note:
1. Only the NOP command is supported during ZQ calibration.
2.CKE must be registered HIGH continuously during the calibration period.
3.All devices connected to the DQ bus should be High-Z during the calibration process.

Figure. ZQ Calibration Short timing



Note:
1. Only the NOP command is supported during ZQ calibration.
2. CKE must be registered HIGH continuously during the calibration period.
3. All devices connected to the DQ bus should be High-Z during the calibration process.

Figure. ZQ Calibration Long timing



Note:
1. Only the NOP command is supported during ZQ calibration.
2. CKE must be registered HIGH continuously during the calibration period.
3. All devices connected to the DQ bus should be High-Z during the calibration process.

Figure. ZQ Calibration Reset timing example

ZQ External Resistor Value, Tolerance and Capacitive Loading

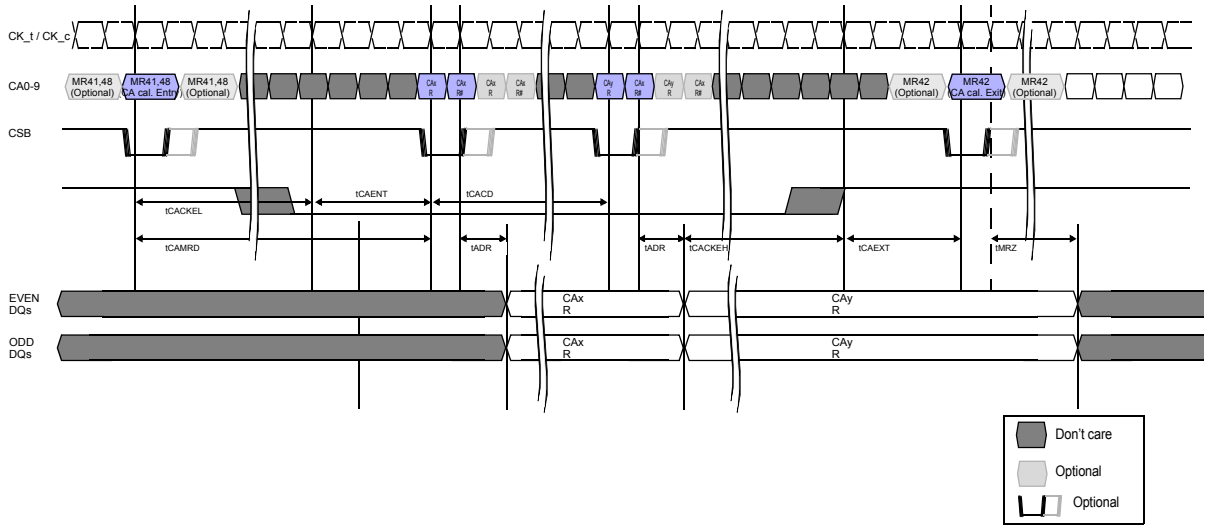
To use the ZQ calibration function, an RZQ ±1% tolerance external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each device or one resistor can be shared between multiple devices if the ZQ calibration timings for each device do not overlap. The total capacitive loading on the ZQ pin must be limited (see the Pin Capacitance table).

Mode Register Write - CA Training Mode

Because CA inputs are Double Data Rate, it may be difficult for memory controller to satisfy CA input setup/hold timings at higher frequency. CA Training mechanism is provided.

CA Training Sequence

a) CA Training mode entry: Mode Register Write to MR#41
b) CA Training session
   Calibrate CA0, CA1, CA2, CA3, CA5, CA6, CA7 and CA8 (see the table "CA to DQ mapping (... #MR41)")
c) CA to DQ mapping change: Mode Register Write to MR#48
d) Additional CA Training session
   Calibrate remaining CA pins (CA4 and CA9) (see the table "CA to DQ mapping (... #MR48)")
e) CA Training mode exit: Mode Register Write to MR#42



Note:

1. Unused DQ must be valid HIGH or LOW during data output period. Unused DQ may transition at the same time as the active DQ. DQS must remain static and not transition.
2. CA to DQ mapping change via MR 48 omitted here for clarity of the timing diagram. Users can select the way enabling MR48 as follows: i) MR41-MR48-MR42, or ii) MR41-MR42 and MR48-MR42. To enable a CA to DQ mapping change, CKE must be driven HIGH prior to issuance of the MRW 48 command. For details, please refer to CA Training Sequence section.
3. Because data out control is asynchronous and will be an analog delay from when all the CA data is available, tADR and tMRZ are defined from CK_t falling edge.
4. It is recommended to hold the CA bus stable for one cycle prior to and one cycle after the issuance of the MRW CA Training Entry Command to ensure setup and hold timings on the CA bus.
5. Optional MRW 41, 48, 42 command and CA calibration command are allowed. To complement these optional commands, optional CS_n assertions are also allowed. All timing must comprehend these optional CS_n assertions:
   a) tADR starts at the falling clock edge after the last registered CS_n assertion.
   b) tCACD, tCACKEL, tCAMRD start with the rising clock edge of the last CS_n assertion.
   c) tCAENT, tCAEXT need to be met by the first CS_n assertion.
   d) tMRZ will be met after the falling clock edge following the first CS_n assertion with exit (MR42) command.
6. CA calibration is not needed before ZQC init if dram is running at a slow (e.g .50MHz) frequency.

The LPDDR3 SDRAM may not properly recognize Mode Register Write command at normal operation frequency before CA Training is finished. Special encodings are provided for CA Training mode enable/disable.
MR#41 and MR#42 encodings are selected so that rising edge and falling edge values are the same. The LPDDR3 SDRAM will recognize MR#41 and MR#42 at normal operation frequency even before CA timing adjustment is finished.
Calibration data will be output through DQ pins. CA to DQ maping is described in the table below.
After timing calibration with MR#41 is finished, users will issue MRW to MR#48 and calibrate remaining CA pins (CA4 and CA9) using DQ0,1,8,9 as calibration data output pins in the table below.

Table. CA Training mode enable (MR#41(29H, 0010 1001B), OP=A4H(1010 0100B))

	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9
Rising Edge	L	L	L	L	H	L	L	H	L	H
Falling Edge	L	L	L	L	H	L	L	H	L	H

Table. CA Training mode disable (MR#42(2AH, 0010 1010B), OP=A8H(1010 1000B))

	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9
Rising Edge	L	L	L	L	L	H	L	H	L	H
Falling Edge	L	L	L	L	L	H	L	H	L	H

Table. CA to DQ mapping (CA Training mode enabled with MR#41)

CA0	CA1	CA2	CA3	CA5	CA6	CA7	CA8	Clock edge
DQ0	DQ2	DQ4	DQ6	DQ8	DQ10	DQ12	DQ14	CK_t rising edge
DQ1	DQ3	DQ5	DQ7	DQ9	DQ11	DQ13	DQ15	CK_t falling edge

Table. CA Training mode enable (MR#48(30H, 0011 0000B), OP=C0H(1100 0000B))

	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9
Rising Edge	L	L	L	L	L	L	L	L	H	H
Falling Edge	L	L	L	L	L	L	L	L	H	H

Table. CA to DQ mapping (CA Training mode enabled with MR#48)

CA4	CA9	Clock edge
DQ0	DQ8	CK_t rising edge
DQ1	DQ9	CK_t falling edge

Note: Other DQs must have valid output (either HIGH or LOW)

Mode Register Write - WR Leveling Mode

In order to provide for improved signal integrity performance, the LPDDR3 SDRAM provides a write leveling feature to compensate for timing skew, affecting timing parameters such as tDQSS, tDSS, and tDSH.

The memory controller uses the write leveling feature to receive feedback from the SDRAM allowing it to adjust the clock to data strobe signal relationship for each DQS_t/DQS_c signal pair. The memory controller performing the leveling must have adjustable delay setting on DQS_t/DQS_c signal pair to align the rising edge of DQS signals with that of the clock signal at the DRAM pin. The DRAM asynchronously feeds back CLK, sampled with the rising edge of DQS signals. The controller repeatedly delays DQS signals until a transition from 0 to 1 is detected. The DQS signals delay established through this exercise ensures the tDQSS specification can be met.

All DQS signals may have to be leveled independantly. During Write Leveling operations each DQS signal latches the clock with a rising strobe edge and drives the result on all DQ[n] of its respective byte.

The LPDDR3 SDRAM enters into write leveling mode when mode register MR2[7] is set HIGH. When entering write leveling mode, the state of the DQ pins is undefined. During write leveling mode, only NOP commands are allowed, or MRW command to exit write leveling operation. Upon completion of the write leveling operation, the DRAM exits from write leveling mode when MR2[7] is reset LOW.

The controller will drive DQS_t LOW and DQS_c HIGH after a delay of tWLDQSEN. After time tWLMRD, the controller provides DQS signal input which is used by the DRAM to sample the clock signal driven from the controller. The delay time tWLMRD(max) is controller dependent. The DRAM samples the clock input with the rising edge of DQS and provides asynchronous feedback on all the DQ bits after time tWLO. The controller samples this information and either increment or decrement the DQS_t and/or DQS_c delay settings and launches the next DQS/DQS# pulse. The sample time and trigger time is controller dependent. Once the following DQS_t/DQS_c transition is sampled, the controller locks the strobe delay settings, and write leveling is achieved for the device. The figure below describes the timing for the write leveling operation.

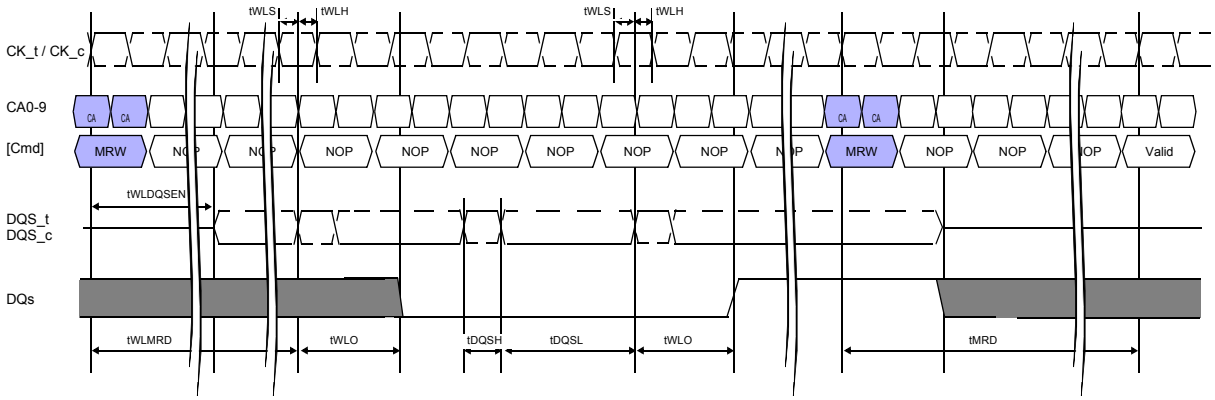


Figure. Write Leveling Timing diagram

Power-down

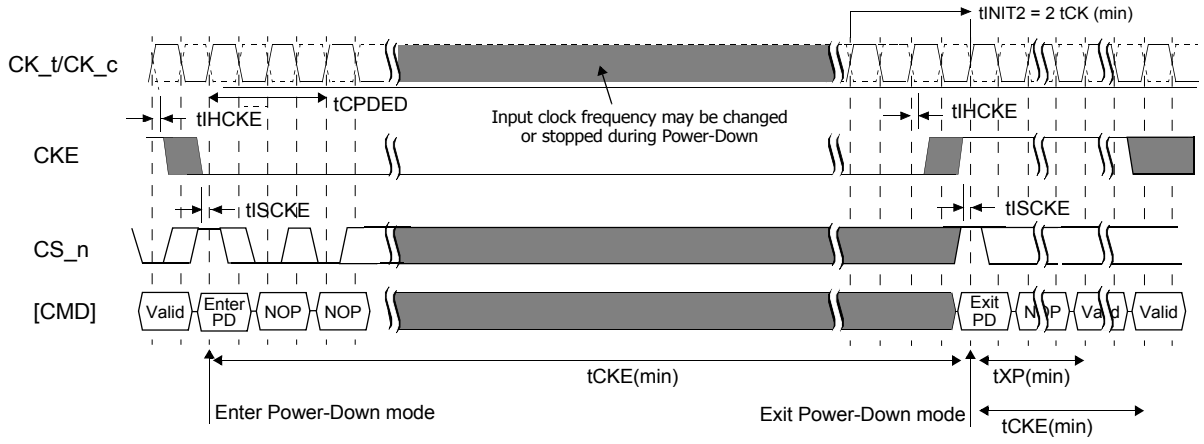
Power-down is entered synchronously when CKE is registered LOW and CS_n is HIGH at the rising edge of clock. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. CKE can go LOW while any other operations such as row activation, PRECHARGE, auto precharge, or REFRESH are in progress, but the power-down IDD specification will not be applied until such operations are complete. Power-down entry and exit are shown in following figures.

Entering power-down deactivates the input and output buffers, excluding CKE. To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW, this timing period is defined as tCPDED. CKE LOW will result in deactivation of input receivers after tCPDED has expired. In power-down mode, CKE must be held LOW; all other input signals are "Don't Care." CKE LOW must be maintained until tCKE,min is satisfied. VREFCA must be maintained at a valid level during power-down.

VDDQ can be turned off during power-down. If VDDQ is turned off, VREFDQ must also be turned off. Prior to exiting power-down, both VDDQ and VREFDQ must be within their respective minimum/maximum operating ranges.

No refresh operations are performed in power-down mode. The maximum duration in power-down mode is only limited by the refresh requirements outlined in the Refresh command section.

The power-down state is exited when CKE is registered HIGH. The controller must drive CS_n HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until tCKE is satisfied. A valid, executable command can be applied with power-down exit latency tXP after CKE goes HIGH. Power-down exit latency is defined in the AC timing parameter table.



Note:

1. Input clock frequency can be changed or the input clock stopped during power-down, provided that the clock frequency is between the minimum and maximum specified frequencies for the speed grade in use, and that prior to power-down exit, a minimum of 2 stable clocks complete.

Figure. Basic power down entry and exit timing diagram

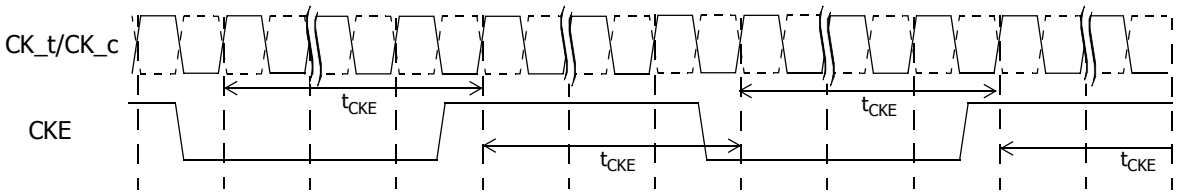
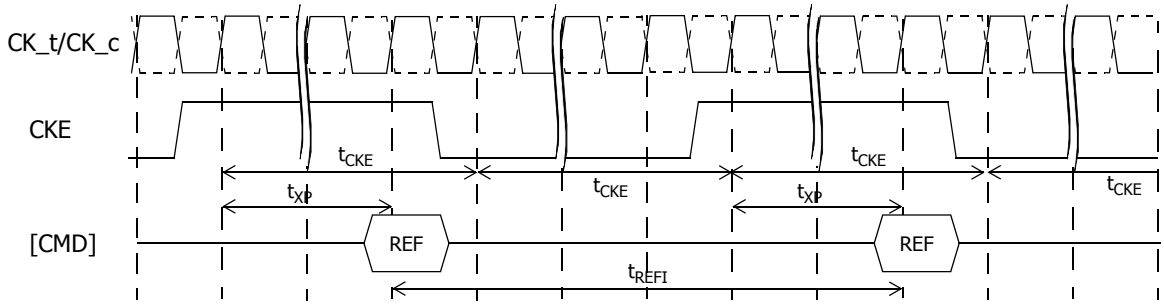
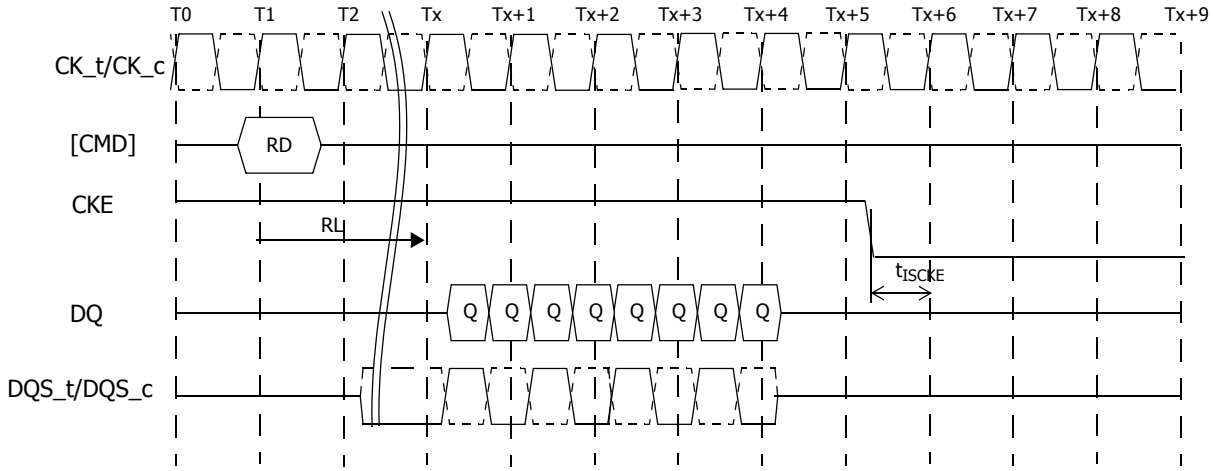


Figure. CKE intensive environment



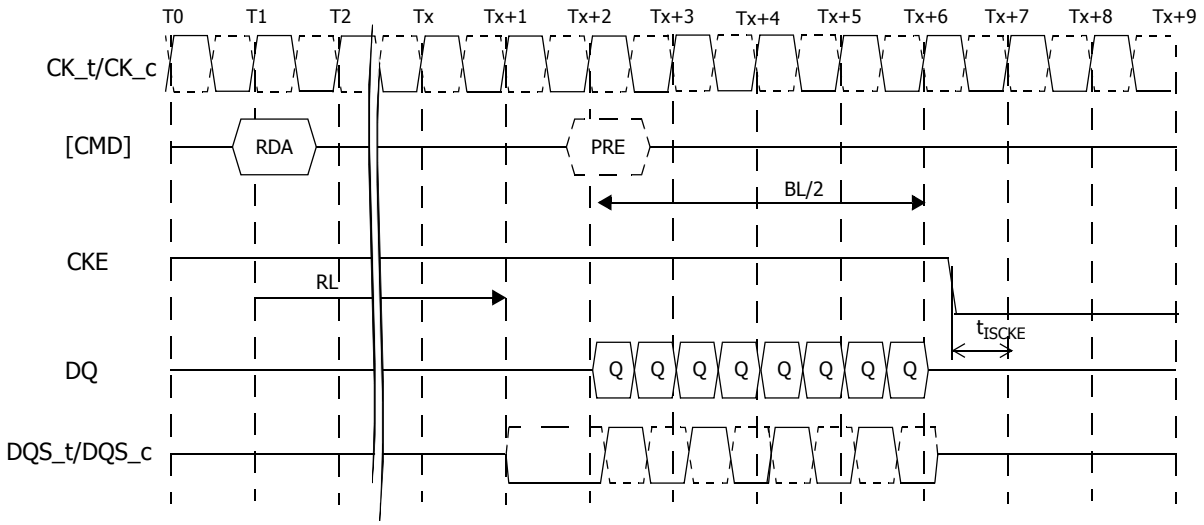
Note:
1. The pattern shown can repeat over an extended period of time. With this pattern, all AC and DC timing and voltage specifications with temperature and voltage drift are ensured.

Figure. REFRESH to REFRESH timing with CKE intensive environment



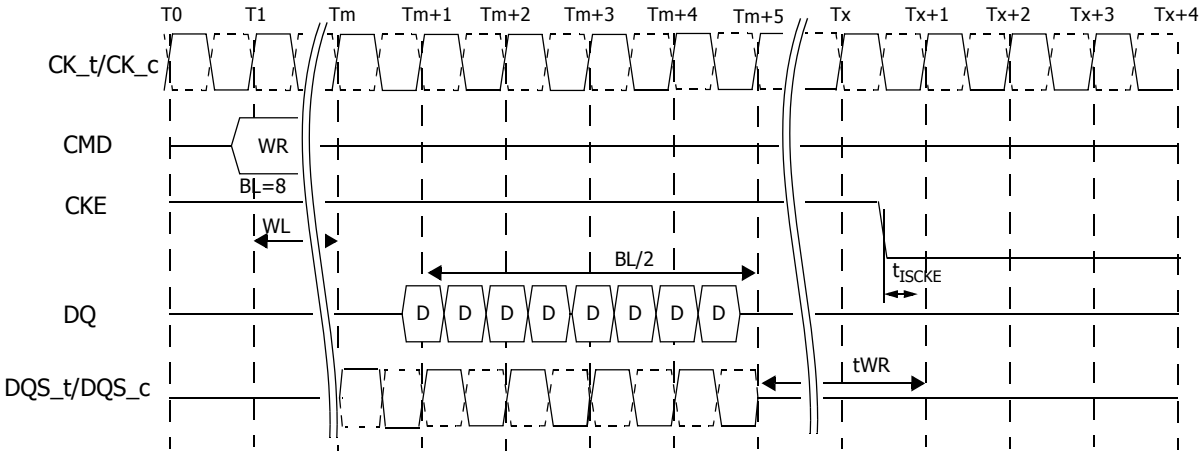
Note:
1. CKE must be held HIGH until the end of the burst operation.
2. CKE can be registered LOW at RL + RU(tDQSCK(MAX)/tCK) + BL/2 + 1 clock cycles after the clock on which the READ command is registered.

Figure. Read to power-down entry



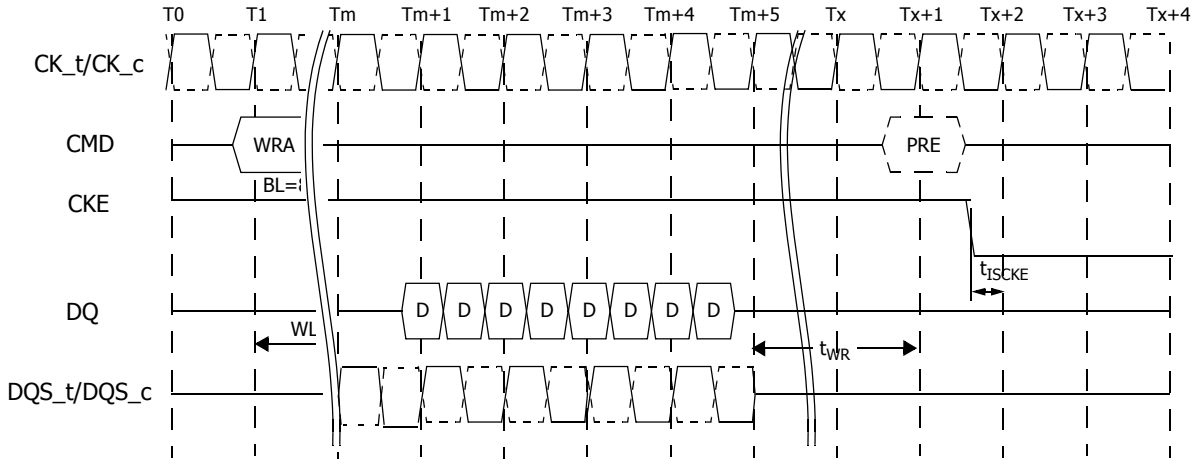
Note:
1. CKE must be held HIGH until the end of the burst operation.
2. CKE can be registered LOW at RL + RU(tDQSCK/tCK)+ BL/2 + 1 clock cycles after the clock on which the READ command is registered.
3. BL/2 with tRTP = 7.5ns and tRAS (MIN) is satisfied.
4. Start internal PRECHARGE.

Figure. Read with Auto Precharge to power-down entry



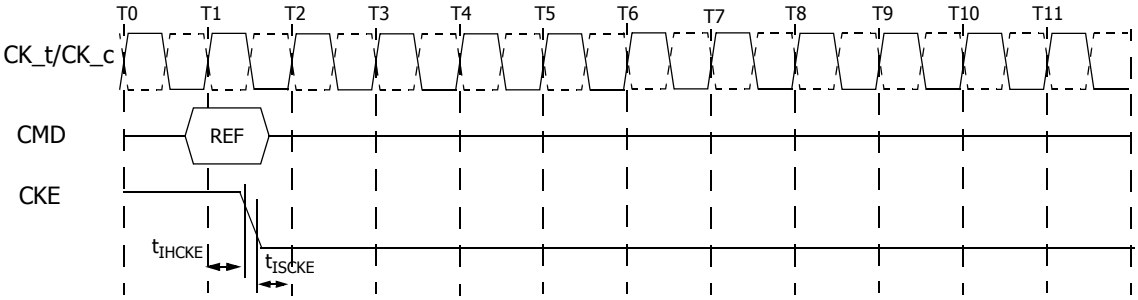
Note:
1. CKE can be registered LOW at WL + 1 + BL/2 + RU(tWR/tCK) clock cycles after the clock on which the WRITE command is registered.

Figure. Write to power-down entry



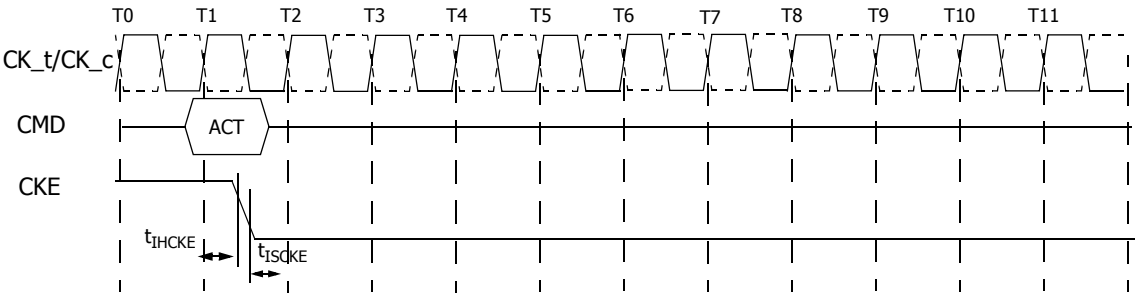
Note:
1. CKE can be registered LOW at WL + 1 + BL/2 + RU(tWR/tCK) + 1 clock cycles after the WRITE command is registered.
2. Start internal PRECHARGE.

Figure. Write with auto precharge to power-down entry



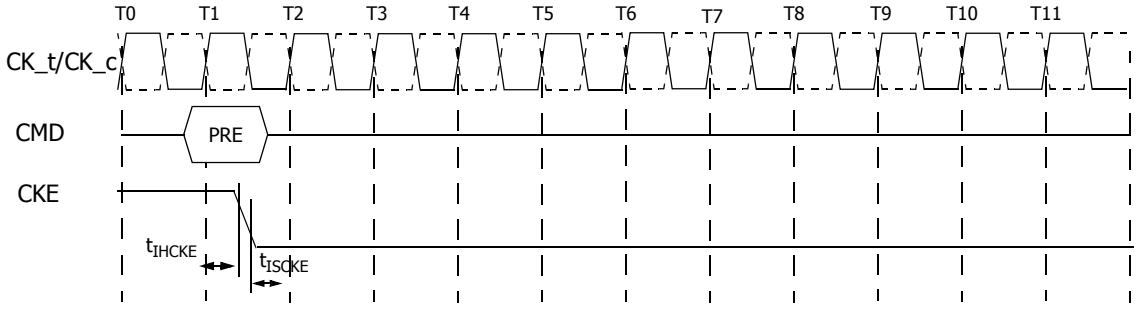
Note.
1. CKE may go LOW tIHCKE after the clock on which the Refresh command is registered.

Figure. Refresh command to power-down entry



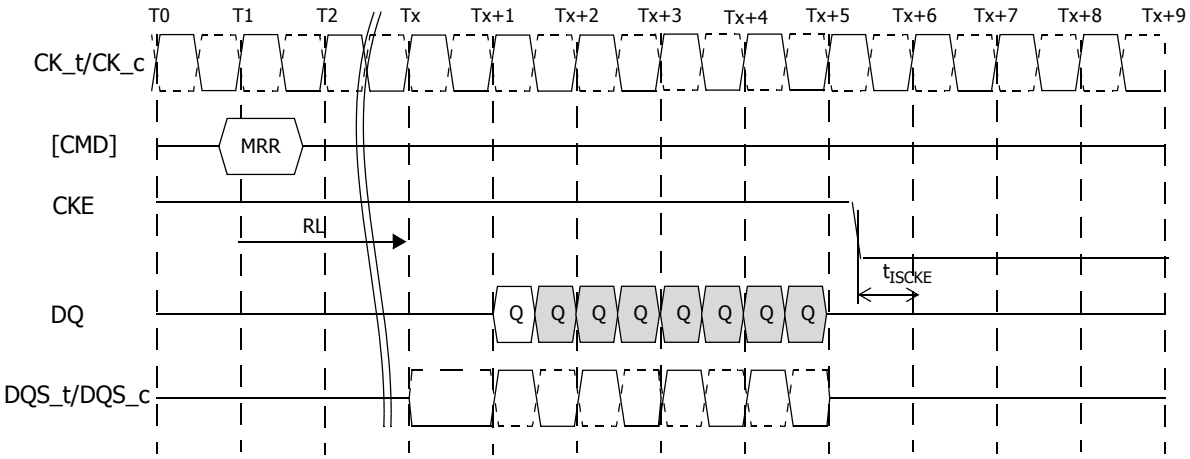
Note.
1. CKE may go LOW tIHCKE after the clock on which the Activate command is registered.

Figure. Activate command to power-down entry



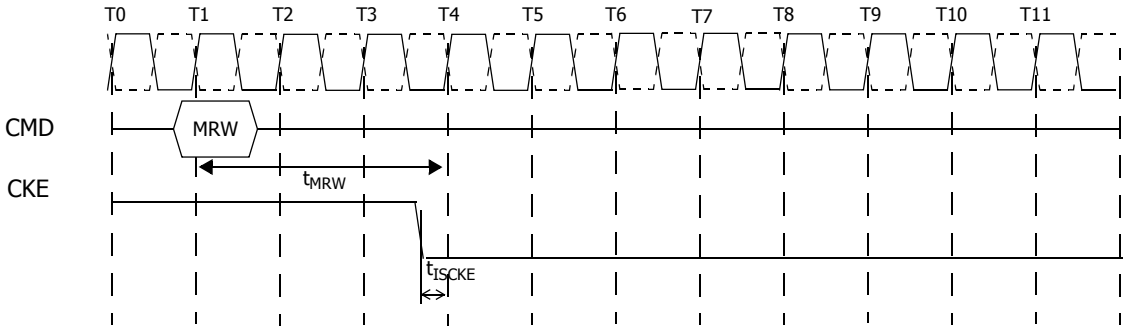
Note. 1. CKE can go LOW tIHCKE after the clock on which the PRECHARGE command is registered.

Figure. Precharge command to power-down entry



Note. 1. CKE can be registered LOW RL + RU(tDQSCK/tCK)+ BL/2 + 1 clock cycles after the clock on which the MRR command is registered.
2. CKE should be held high until the end of the burst operation.

Figure. MRR to power-down entry



Note. 1. CKE may be registered LOW tMRW after the clock on which the Mode Register Write command is registered.

Figure. MRW command to power-down entry

Deep Power Down

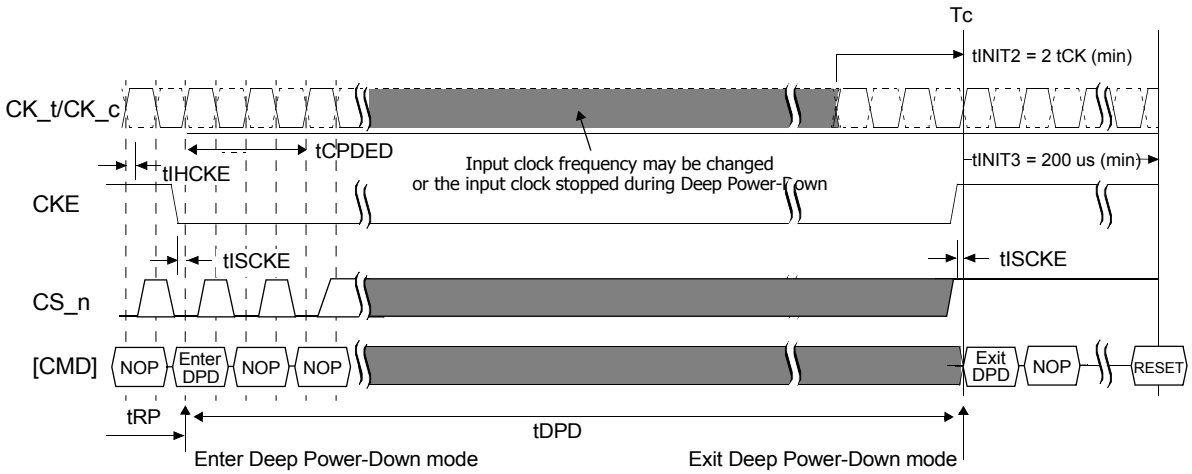
Deep Power-Down is entered when CKE is registered LOW with CS_n LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of clock. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress.

All banks must be in idle state with no activity on the data bus prior to entering the Deep Power Down mode. During Deep Power-Down, CKE must be held LOW.

In Deep Power-Down mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry may be disabled within the SDRAM. All power supplies must be within specified limits prior to exiting Deep Power-Down. VrefDQ and VrefCA may be at any level within minimum and maximum levels (see Abolute Maximum Ratings). However prior to exiting Deep Power-Down, Vref must be within specified limits (See Recommended DC Operating Conditions).

The contents of the SDRAM will be lost upon entry into Deep Power-Down mode.

The Deep Power-Down state is exited when CKE is registered HIGH, while meeting tISCKE with a stable clock input. The SDRAM must be fully re-initialized as described in the Power up initialization Sequence. The SDRAM is ready for normal operation after the initialization sequence. The SDRAM is ready for normal operation after the initialization sequence is completed.



Note:

1. Initialization sequence may start at any time after Tc.
2. tINIT3, and Tc refer to timings in the LPDDR3 initialization sequence. For more detail, see Power-Up and Initialization.
3. Input clock frequency may be changed or the input clock stopped during deep power-down, provided that upon exiting deep power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to deep power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

Figure. Deep power down entry and exit timing diagram

Input clock stop and frequency change

LPDDR3 devices support input clock frequency change during CKE LOW under the following conditions:
• tCK(abs)min is met for each clock cycle;
• Refresh Requirements apply during clock frequency change;
• During clock frequency change, only REFab or REFpb commands may be executing;
• Any Activate or Precharge commands have executed to completion prior to changing the frequency;
• The related timing conditions (tRCD, tRP) have been met prior to changing the frequency;
• The initial clock frequency shall be maintained for a minimum of 3 clock cycles after CKE goes LOW;
• The clock satisfies tCH(abs) and tCL(abs) for a minimum of 2 clock cycles prior to CKE going HIGH.
After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR3 devices support clock stop during CKE LOW under the following conditions:
• CK_t is held LOW and CK_c is held HIGH during clock stop;
• Refresh Requirements apply during clock stop;
• During clock stop, only REFab or REFpb commands may be executing;
• Any Activate or Precharge commands have executed to completion prior to stopping the clock;
• The related timing conditions (tRCD, tRP) have been met prior to stopping the clock;
• The initial clock frequency shall be maintained for a minimum of 3 clock cycles after CKE goes LOW;
• The clock satisfies tCH(abs) and tCL(abs) for a minimum of 2 clock cycles prior to CKE going HIGH.

LPDDR3 devices support input clock frequency change during CKE HIGH under the following conditions:
• tCK(abs)min is met for each clock cycle;
• Refresh Requirements apply during clock frequency change;
• Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
• The related timing conditions (tRCD, tWR, tRP, tMRW, tMRR, etc.) have been met prior to changing the frequency;
• CS_n shall be held HIGH during clock frequency change;
• During clock frequency change, only REFab or REFpb commands may be executing;
• The LPDDR3 device is ready for normal operation after the clock satisfies tCH(abs) and tCL(abs) for a minimum of 2tCK + tXP.
After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR3 devices support clock stop during CKE HIGH under the following conditions:
• CK_t is held LOW and CK_c is held HIGH during clock stop;
• CS_n shall be held HIGH during clock stop;
• Refresh Requirements apply during clock stop;
• During clock stop, only REFab or REFpb commands may be executing;
• Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock;
• The related timing conditions (tRCD, tWR, tRP, tMRW, tMRR, etc.) have been met prior to stopping the clock;
• The LPDDR3 device is ready for normal operation after the clock is restarted and satisfies tCH(abs) and tCL(abs) for a minimum of 2tCK + tXP.

No Operation command

The purpose of the No Operation command (NOP) is to prevent the LPDDR3 device from registering any unwanted command
between operations. Only when the CKE level is constant for clock cycle N-1 and clock cycle N, a NOP command may be issued at
clock cycle N. A NOP command has two possible encodings:
1. CS_n HIGH at the clock rising edge N.
2. CS_n LOW and CA0, CA1, CA2 HIGH at the clock rising edge N.
The No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.