SK Hynix UFS Product Family
UFS 2.1 Compatible

1.0 Version.

Copyright and Proprietary Information Notice

The information contained in this datasheet is confidential and proprietary to SK hynix, Inc. No part of this datasheet may be distributed or disclosed to any third party & reproduced or translated in any form, without written permission of SK hynix, Inc.

The information in this document may be changed with notice by providing updated version of the document.

For updates or additional information about SK hynix, Inc. UFS products, contact your convenient SK hynix office.

All brand names, trademarks and registered trademarks belong to their respective owners.

SK hynix, Inc.
http://www.skhynix.com/en/index.jsp

@2016 **SK hynix**, Inc. All rights reserved.

Revision History

Revision No.	History	Draft Date	Remark
0.1	First draft version	Jan. 25, 2016	
1.0	Customer sample datasheet released	Mar. 31, 2016	

Table of Contents

1. SK hynix UFS Introduction 6
1.1 General Description 6
1.2 Product Line-up 6
1.3 Key Features 6
1.4 UFS Architecture 7
1.5 UFS System Model 8

2. Package Configurations 9
2.1 Package Ball Map 9
2.2 Pin Description 10
2.3 Package Mechanical Drawing 11
2.4 Connection Guide 13

3. UFS Characteristics 14
3.1 Performance 14
3.2 Power 15
3.3 Temperature & Humidity 18
3.4 Bandwidth 18
3.5 User Density Size 19
3.6 Device LU Partitioning 19

4. UFS Feature Notes 20
4.1 FFU 20
4.2 Supported VPD Pages 22
4.3 Mode Page 22

5. UFS General Parameters 23
5.1 Power Supplies 23
5.2 Reset Signal 23
5.3 Reference Clock 24
5.4 Bus Signal Levels 26
5.5 PCB Guideline 28

6. Latency Time 29

7. UPIU Transaction Codes 30
7.1 UFS SCSI Command 30

8. UFS Descriptors, Flags, Attributes 31
8.1 Device Descriptor 32
8.2 Geometry Descriptor 34
8.3 Unit Descriptor 37
8.4 Power Parameters Descriptor 40
8.5 Interconnect Descriptor 42
8.6 Manufacturer Name String Descriptor 42
8.7 Product Name String Descriptor 43
8.8 OEM ID String Descriptor 43
8.9 Serial Number String Descriptor 43
8.10 Product Revision Level String Descriptor 44
8.11 Device Health Descriptor 44
8.12 UFS Flags 46
8.13 UFS Attributes 48

9. M-PHY & UniPro Attributes 52
9.1 M-TX Capacity Attributes 52
9.2 M-RX Capacity Attributes 55
9.3 M-TX Configuration Attributes 59
9.4 M-RX Configuration Attributes 63
9.5 M-TX & M-RX Status Attributes 64
9.6 UniPro L1.5 Attributes 65
9.7 UniPro L2 Attributes 70
9.8 UniPro L3 Attributes 71
9.9 UniPro L4 Attributes 71
9.10 UniPro DME DDB L1 Attributes 72
9.11 UniPro TstSrc/TstDst Attributes 73

1. SK hynix UFS Introduction

1.1 General Description

SK hynix UFS product consists of NAND flash and UFS controller.
UFS has the built-in intelligent controller which manages interface protocols, wear leveling, bad block management, garbage collection, and ECC. UFS protects data contents from sudden power off. The first UFS of SK hynix is compatible with JEDEC standard UFS2.1 specification and supports UniPro v1.6 and M-PHY v3.0 (HS-G1/G2/G3 Rate A/B, PWM-G1/G2/G3/G4/G5, Dual-lane)

1.2 Product Line-up

Density	Part Number	NAND Stack	PKG size (mm)	Package Type
32GB	H28U62301AMR	128Gb x 2	11.5 x 13 x 1.0	153FBGA
64GB	H28U74301AMR	128Gb x 4	11.5 x 13 x 1.0	
128GB	H28U88301AMR	128Gb x 8	11.5 x 13 x 1.0	

1.3 Key Features

- **UFS2.1 compatible**
  - backward compatibility with UFS2.0

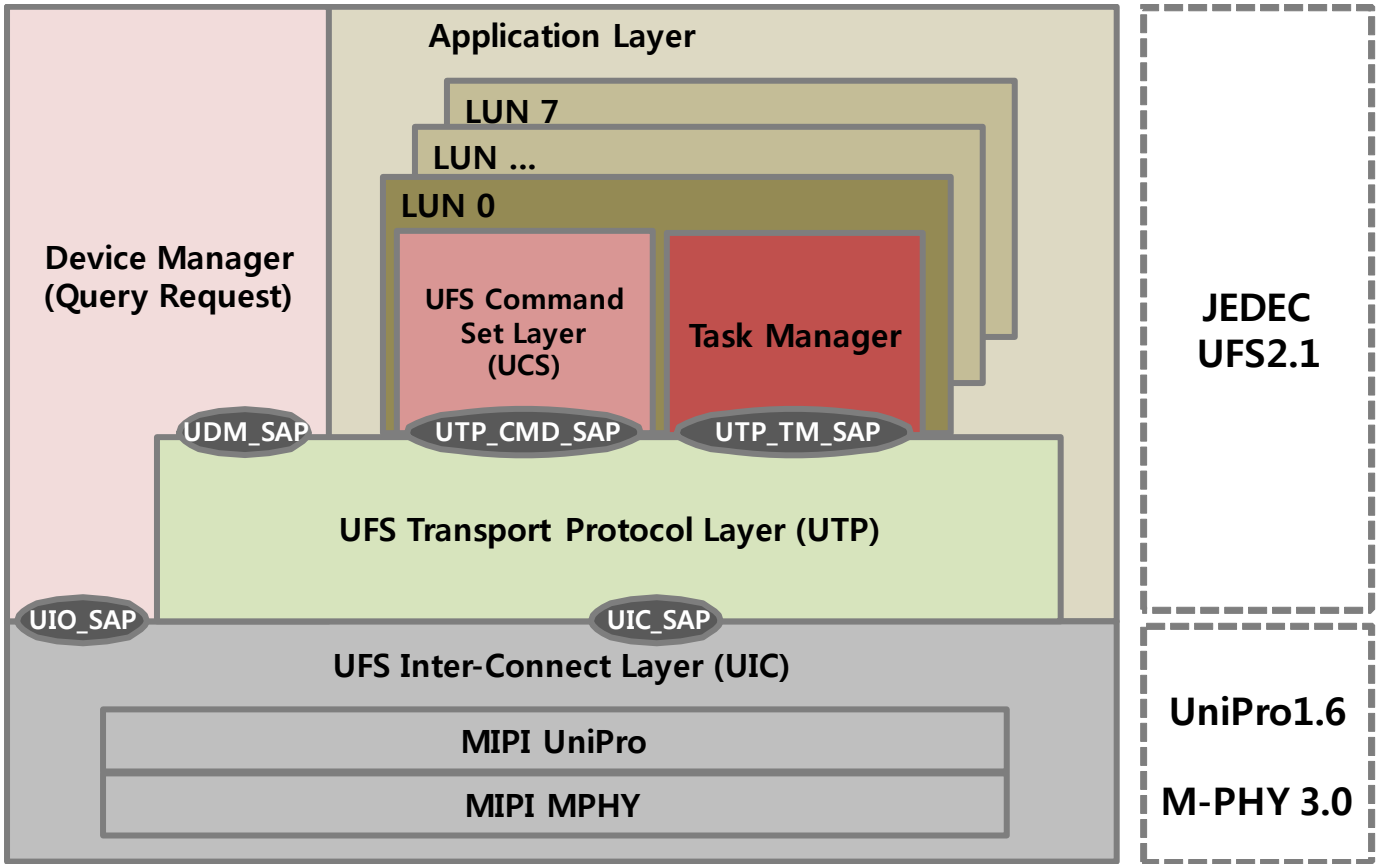
- **Operating Voltage Range**
  - V_{cc} (NAND) : 2.7V - 3.6V
  - V_{ccq} (CTRL) : Not Used
  - V_{ccq2} (CTRL) : 1.7V - 1.95V

- **Temperature**
  - Operation Temperature (-25℃ ~ +85℃)
  - Storage Temperature (-40℃ ~ +85℃)

- **Reference**
  - JEDEC UFS Specification V2.1
  - MIPI UniPro Specification V1.6
  - MIPI M-PHY Specification V3.0

- **Supported Features**
  - Erase / Discard / Purge / Wipe
  - PWM G1~G5 / HS-G1~G3
  - HS-G3 1L/2L
  - Command Queuing / Cache
  - RPMB / BOOT LU
  - Power-on/HW/EndPoint/LU Reset
  - BKOP
  - High Priority LU
  - Reliable Write Operation
  - Write Protect
  - Task Management operations
  - Context ID, Data Tag
  - Secure Removal Type
  - Power Management operations
  - MAX 8LU supported
  - Device Health Descriptor
  - Field Firmware Update

1.4 UFS Architecture

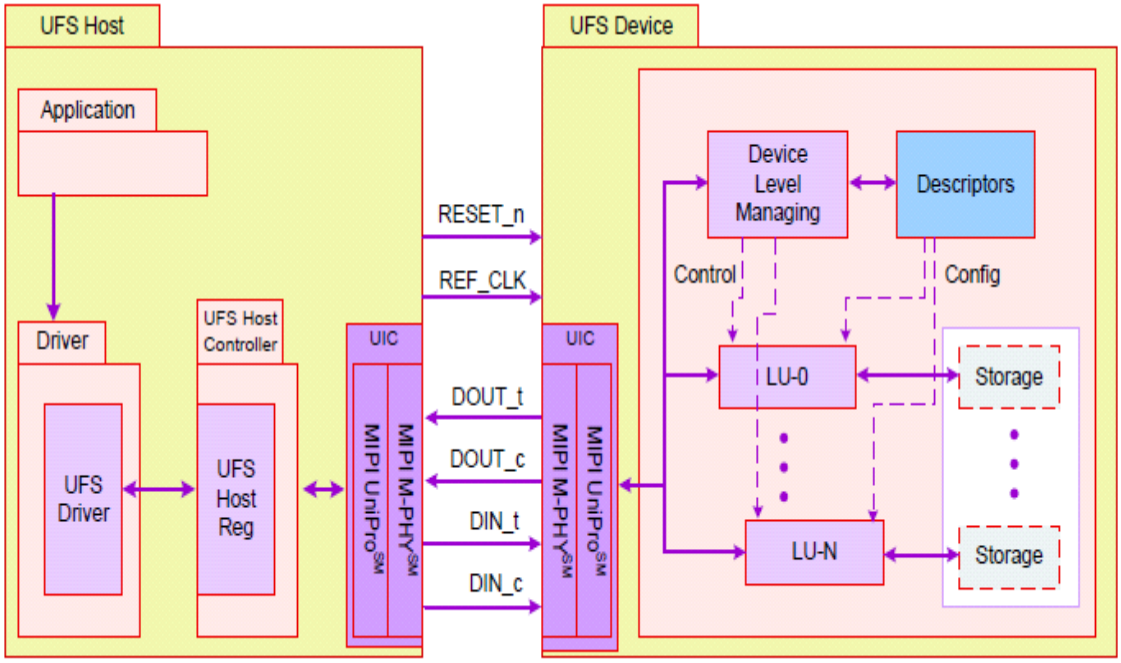


1.4.1 Reference Documents

1) JEDEC STANDARD Universal Flash Storage (UFS) Version 2.1 _ JESD220C _ Mar. 2016
2) MIPI Alliance M-PHY Version 3.0 _ 26 Jul. 2013
3) MIPI Alliance Unified Protocol (UniPro) Version 1.6 _ 6 Aug. 2013
4) SAM, SCSI Architecture Model-5 (SAM-5), Revision 05, 19 May 2010
5) SPC, SCSI Primary Commands-4 (SPC-4), Revision 27, 11 Oct. 2010
6) SBC, SCSI Block Commands-3 (SBC-3) Revision 24, 05 Aug. 2010

1.5 UFS System Model

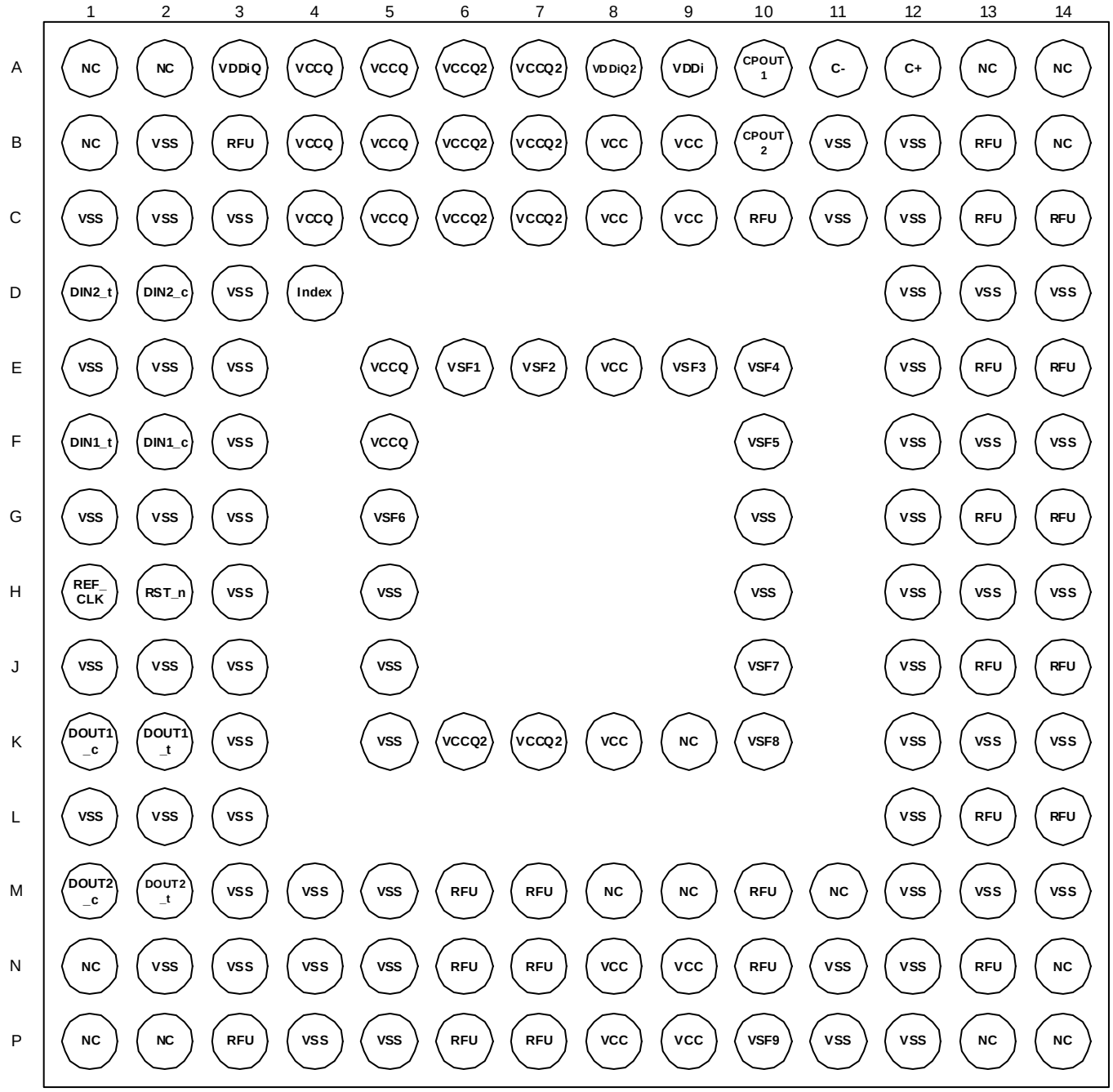
The Figure1 shows an example of UFS system. It shows how an UFS host is connected to an UFS device, the position of UFS host controller and its related UFS HCI interface



[Figure 1] UFS System Model

2. Package Configurations

2.1 Package Ball Map



[Figure 2] FBGA153 Package Connection (Top view through Package)

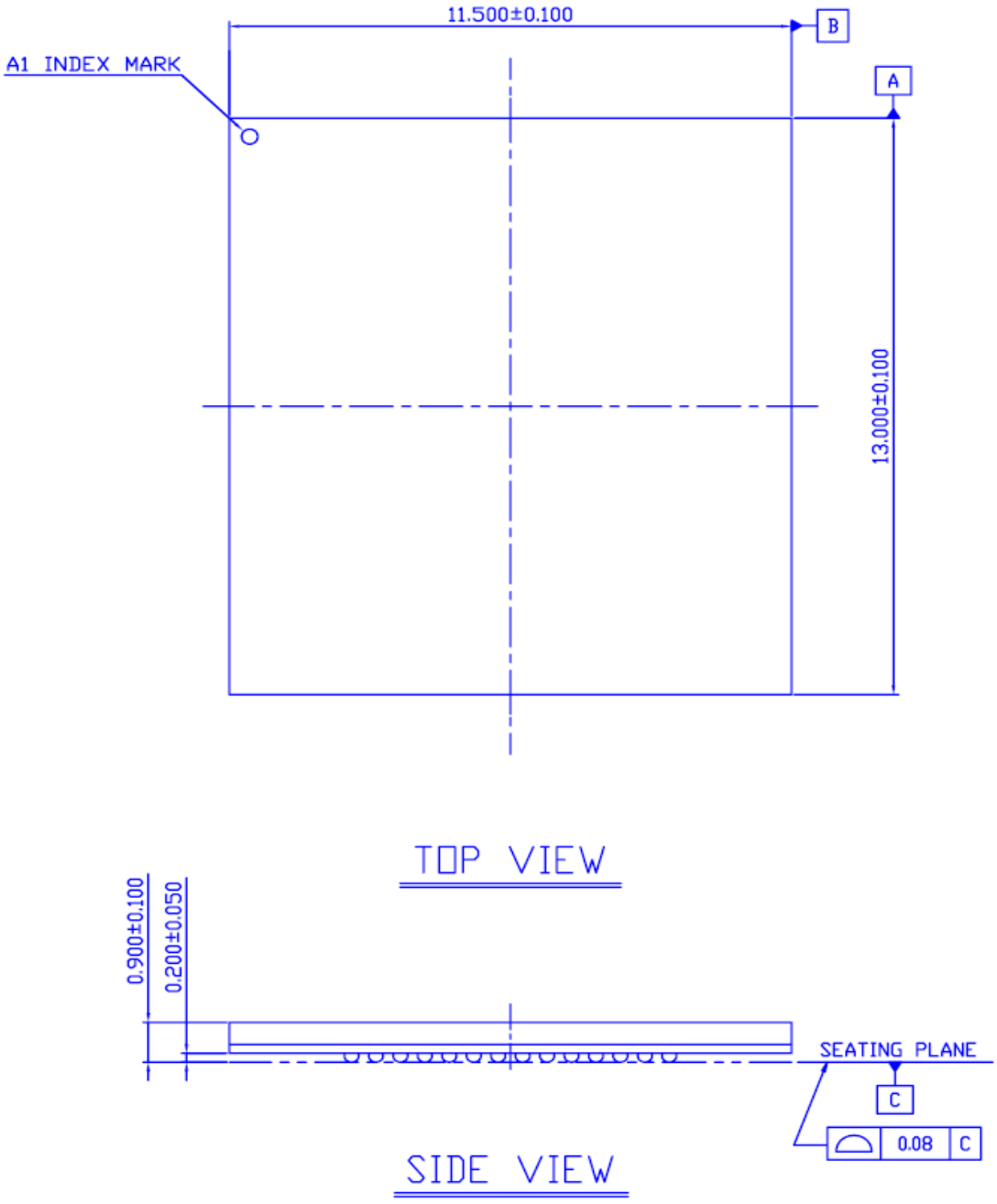
2.2 Pin Description

Name	Type	Pin No.	Description
V_{cc}	Supply	B8~9, C8~9, E8, K8, N8~9, P8~9	3.3V supply voltage for the memory devices
V_{ccq}	Supply	A4~5, B4~5, C4~5, E5, F5	1.2V supply voltage for the memory controller Not used internally for SK hynix's UFS2.1
V_{ccq2}	Supply	A6~7, B6~7, C6~7, K6~7	1.8V supply voltage for the memory controller
VDDi	Input	A9	Input terminal to provide bypass capacitor for internal regulator
VDDiQ	Input	A3	Input terminal to provide bypass capacitor for internal regulator
VDDiQ2	Input	A8	Input terminal to provide bypass capacitor for internal regulator. Connect 1μF capacitor from VDDiQ2 to ground.
Vss	Supply	B2, B11~12, C1~3, C11~12, D3, D12~14, E1~3, E12, F3, F12~14, G1~3, G10, G12, H3, H5, H10, H12~14, J1~3, J5, J12, K3, K5, K12~14, L1~3, L12, M3~5, M12~14, N2~5, N11~12, P4~5, P11~12	Supply voltage ground
RST_n	Input	H2	Input hardware reset signal. This is an active low signal.
REF_CLK	Input	H1	Input reference clock
DIN1_t DIN1_c	Input	F1 / F2	Downstream data lane 1. Differential input signals into UFS device from the host. DIN1_t is the positive node of the differential signal pair.
DIN2_t/ DIN2_c	Input	D1 / D2	Downstream data lane 2. Differential input signals into UFS device from the host.
DOUT1_t/ DOUT1_c	Output	K2 / K1	Upstream data lane 1. Differential output signals from the UFS device to the host. DOUT1_t is the positive node of the differential signal pair.
DOUT2_t/ DOUT2_c	Output	M2 / M11	Upstream data lane 2. Differential output signals from the UFS device to the host.
C+/C-	Input	A12 / A11	Optional charge pump capacitor terminal. Not used internally for SK hynix's UFS2.1
CPOUT1/ CPOUT2	Input	A10 / B10	Optional charge pump output capacitor terminal. Not used internally for SK hynix's UFS2.1
NC	Input		No connect
RFU	-		Reserved for Future Use
VSF	-	E6, E7, E9, E10, F10, G5, J10, K10, P10	Vendor Specific Function. SK hynix uses G5, E10, K10, P10 as VSF pin

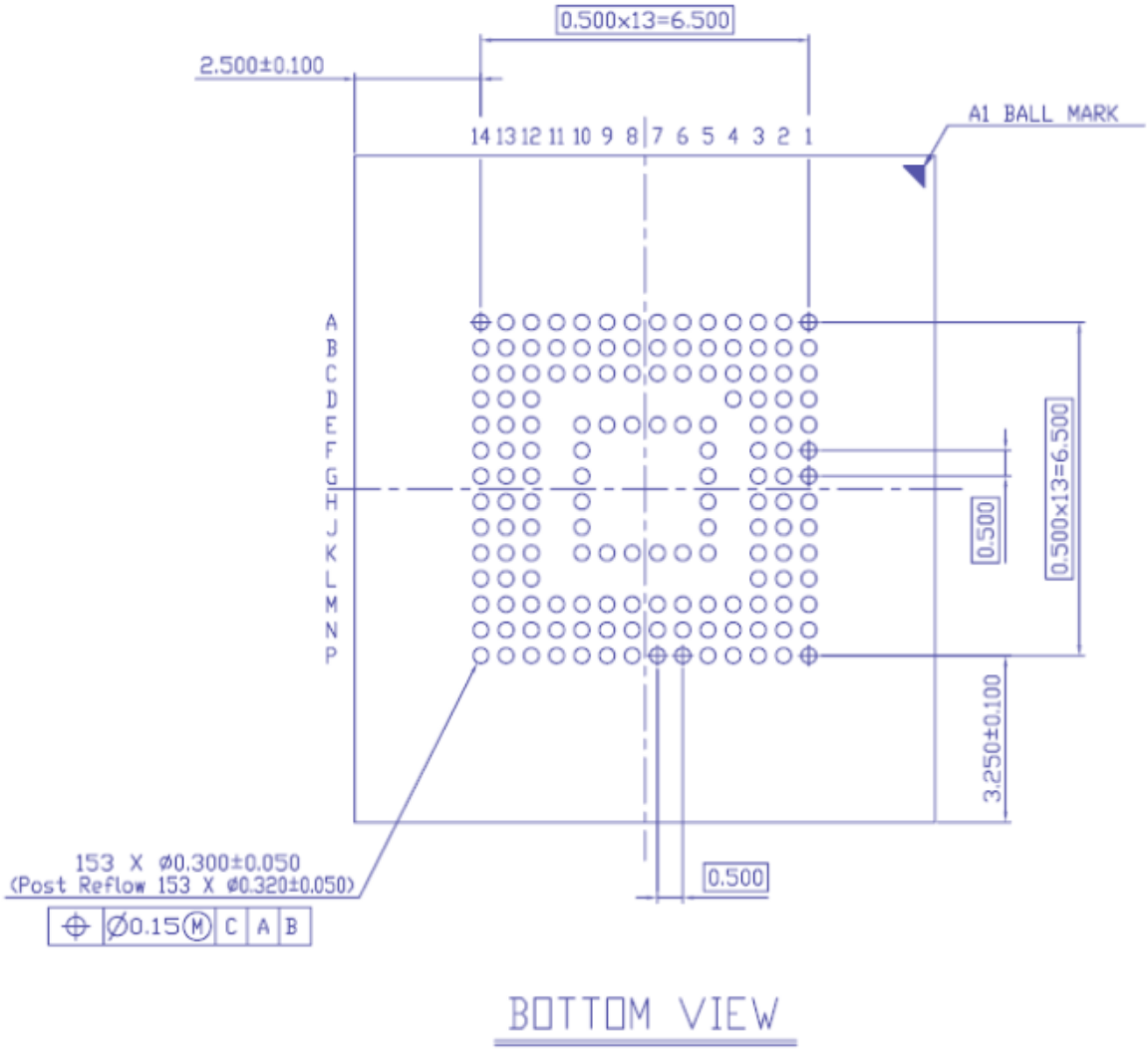
[Table 1] FBGA153 Pin Description

2.3 Package Mechanical Drawing

■ **11.5mm x 13.0mm x Tmm**

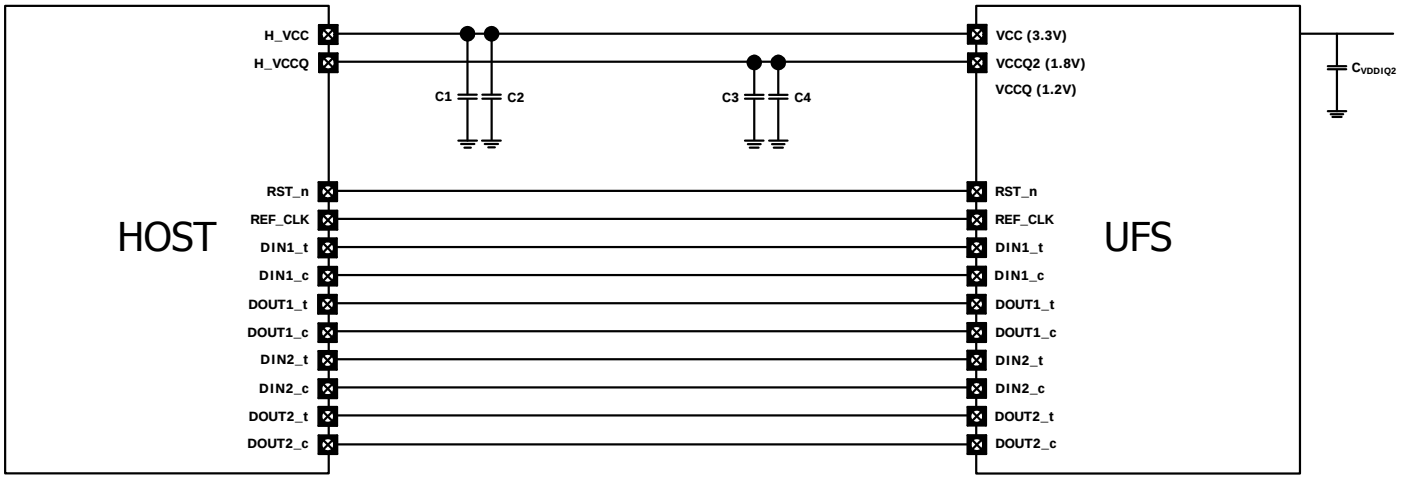


[Figure 3-1] Package Dimension Top and Side



[Figure 3-2] Package Dimension Bottom

2.4 Connection Guide



[Figure 3-3] Connection guide Diagram

• If Host does not support 2nd lane, 2nd signal lines (DIN2_t, DIN2_C, DOUT2_t, DOUT2_C) are floating

[Unit : µF]

Parameter	Symbol	Min	Max	Recommend	Remark
V_{cc} (3.3V)	C_1	1	10	4.7	Coupling cap should be connected with V_{cc} and Vss as closely as possible
	C_2	0.1		0.1	
V_{ccq2} (1.8V)	C_3	1	4.7	4.7	Coupling cap should be connected with V_{ccq2} and Vss as closely as possible
	C_4	0.1		0.1	
VDDiQ2	C_{VDDiQ2}	1	4.7	1	Coupling cap should be connected with VDDiQ2 and Vss as closely as possible

[Table 2] Connection guide specification

3. UFS Characteristics

3.1 Performance

Density	Sequential (MB/s)				Test Condition
	Read		Write		
	QD = 1	QD = 4	QD = 1	QD = 4	
32GB	420	520	125	125	HS-G2B 2L Fast Mode
64GB	420	520	200	200	
128GB	420	520	200	200	
32GB	420	520	125	125	HS-G3B 1L Fast Mode
64GB	420	520	200	200	
128GB	420	520	200	200	
32GB	420	760	125	125	HS-G3B 2L Fast Mode
64GB	420	800	200	200	
128GB	420	800	200	200	

- Device level test without file system overhead
- Seq. Chunk size : 512KB
- Enabled feature : Cache on

3.2 Power

UFS Power Mode Management

UFS Power Mode	Unipro Power Mode	M-PHY Power Mode	V_{cc} Power	V_{ccq2} Power
Active	FAST_STATE	HS-BURST	On	On
Idle	SLEEP_STATE	STALL	On	On
Idle2	HIBERNATE_STATE	HIBERN8	On	On
Sleep	HIBERNATE_STATE	HIBERN8	Off[1)]	On
PowerDown	OFF_STATE	UNPOWERED	Off[1)]	Off[1)]

• NOTE 1 Host can turn off the power for power consumption reduction

3.2.1 Active Power Mode

	Density		Room Temperature = 25℃	
			I_{CC}	I_{CCQ2}
HS-G3-1L	32GB (DDP)	Avg.	100mA	240mA
		Peak	280mA	500mA
	64GB (QDP)	Avg.	100mA	240mA
		Peak	280mA	500mA
	128GB (ODP)	Avg.	100mA	240mA
		Peak	300mA	520mA
HS-G3-2L	32GB (DDP)	Avg.	100mA	290mA
		Peak	280mA	500mA
	64GB (QDP)	Avg.	100mA	290mA
		Peak	280mA	500mA
	128GB (ODP)	Avg.	100mA	300mA
		Peak	300mA	580mA

• V_{cc} = 3.3V, V_{ccq2} = 1.8V, V_{ccq} Not Used Internally
• HS-G3B 2L Fast Mode, Not 100% tested
• The measurement for max RMS current is the average RMS current consumption over a period of 100ms
• Peak current is measured at 20μs resolution.

3.2.2 Idle Power Mode

Density	Room Temperature = 25℃	
	I_{CC}	I_{CCQ2}
32GB (DDP)	40uA	110mA
64GB (QDP)	80uA	110mA
128GB (ODP)	160uA	110mA

- V_{cc} = 3.3V, V_{ccq2} = 1.8V, V_{ccq} Not Used Internally
- HS-G3B 2L Fast Auto Mode, Not 100% tested

3.2.3 Idle2 Power Mode

Density	Room Temperature = 25℃		Hot Temperature = 85℃	
	I_{CC} (Typ.)	I_{CCQ2} (Typ.)	I_{CC} (Max)	I_{CCQ2} (Max)
32GB (DDP)	40μA	400μA	100μA	5mA
64GB (QDP)	80μA	400μA	200μA	5mA
128GB (ODP)	160μA	400μA	400μA	5mA

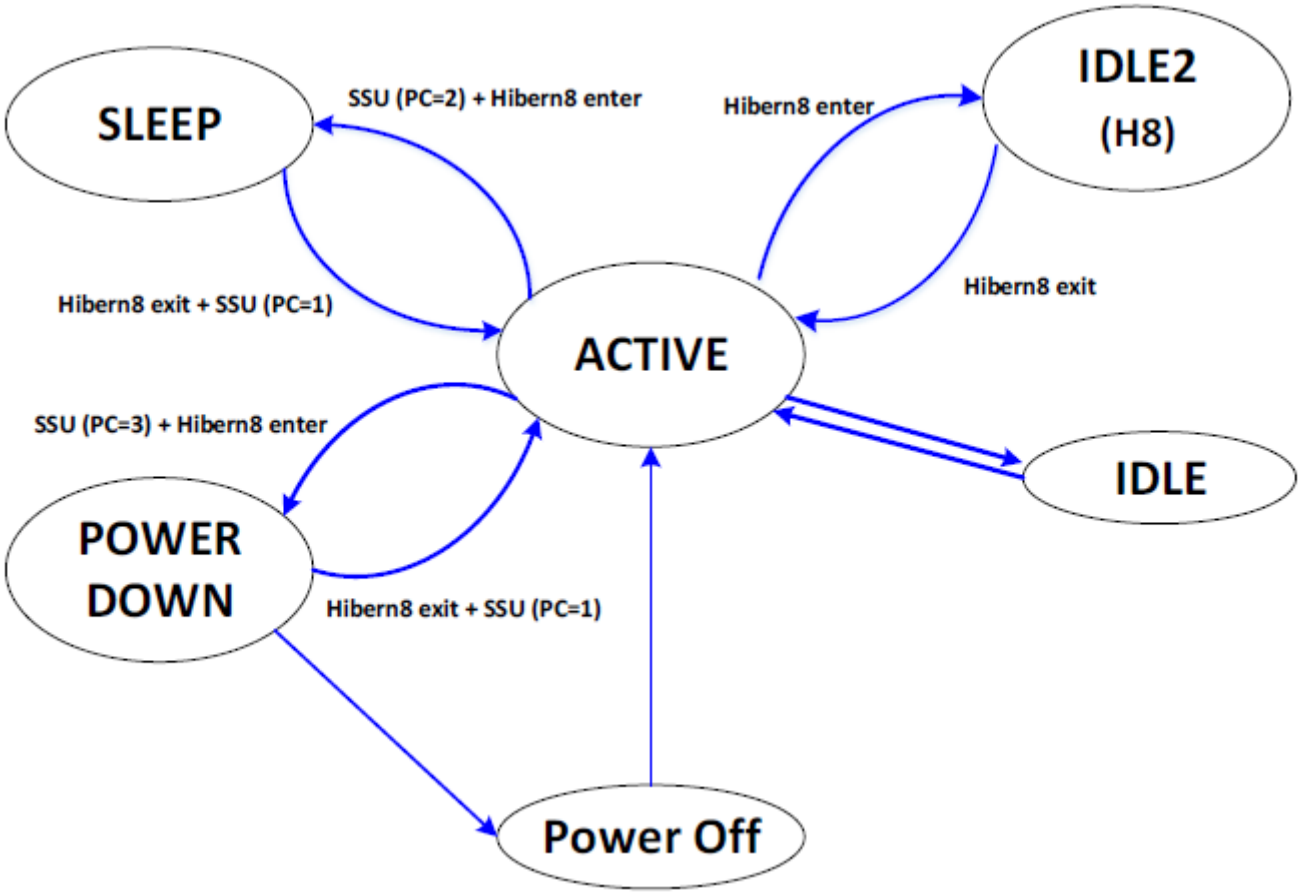
- Host shall issue "HIBERN8 Enter" to enter Idle2 power mode.
- Not 100% tested

3.2.4 Sleep Power Mode

Density	Room Temperature = 25℃		Hot Temperature = 85℃	
	I_{CC} (Typ.)	I_{CCQ2} (Typ.)	I_{CC} (Max)	I_{CCQ2} (Max)
32GB (DDP)	0μA	400μA	0μA	5mA
64GB (QDP)	0μA	400μA	0μA	5mA
128GB (ODP)	0μA	400μA	0μA	5mA

- Host shall issue SSU(Sleep) and "HIBERN8 Enter" to enter Sleep
- V_{cc} Off (V_{cc} = 0V)
- Not 100% tested

3.2.5 UFS Power Mode Transition Diagram



[Figure 4] Power mode state

- Host shall issue "Hibern8 enter" to enter Idle2 power mode.
- In Sleep power mode, V_{cc} can turned off to reduce power consumption.
- In PowerDown power mode, both V_{cc} and V_{ccq2} can turned off.

3.3 Temperature & Humidity

3.3.1 Temperature Condition

Density	Temperature	Remark
Operation Temperature	-25℃ ~ 85℃	-
Storage Temperature	-40℃ ~ 85℃	-

• Operation Temperature is the UFS case surface temperature on the center of top side of the case

3.3.2 Humidity Condition

Density	Humidity	Remark
Operation Humidity	0% RH ~ 95% RH (Non-Condensing)	-
Storage Humidity	0% RH ~ 95% RH (Non-Condensing)	-

3.4 Bandwidth

Bandwidth	Description	Remark
PWM-G1	3 ~ 9 Mbps	Mandatory
PWM-G2	6 ~ 18 Mbps	Mandatory
PWM-G3	12 ~ 36 Mbps	Mandatory
PWM-G4	24 ~ 72 Mbps	Mandatory
PWM-G5	48 ~ 144 Mbps	Optional (Supported)
PWM-G6	96 ~ 288 Mbps	Optional (Not Supported)
PWM-G7	192 ~ 576 Mbps	Optional (Not Supported)
HS-G1	Rate A = 1248 Mbps (19.2/38.4/26/52MHz) Rate B = 1459.2 Mbps (19.2/38.4MHz) 1456 Mbps (26/52 MHz)	Mandatory
HS-G2	Rate A = 2496 Mbps (19.2/38.4/26/52MHz) Rate B = 2918.4 Mbps (19.2/38.4MHz) 2912 Mbps (26/52 MHz)	Mandatory
HS-G3	Rate A = 4992 Mbps (19.2/38.4/26/52MHz) Rate B = 5836.8 Mbps (19.2/38.4MHz) 5824 Mbps (26/52 MHz)	Optional (Supported)

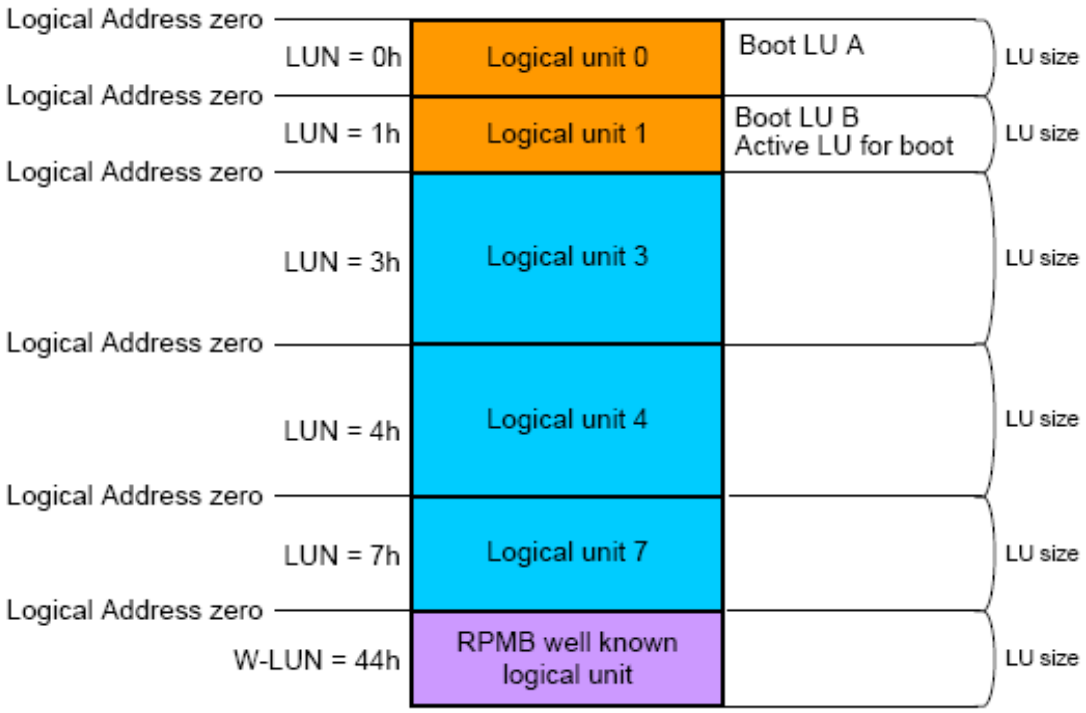
3.5 User Density Size

Capacity	User Density	Ratio	qTotalRawDeviceCapacity (Hex)
32GB	29.80GB	93.1%	0x3B9E000
64GB	59.60GB	93.1%	0x7734000
128GB	119.17GB	93.1%	0xEE60000

• User Density and Ratio are the values before LU configuration

3.6 Device LU Partitioning

UFS Device shall support up to 8 Logical Units and one RPMB LU. Two of 8 Logical Units can be configured as boot LU A & B.



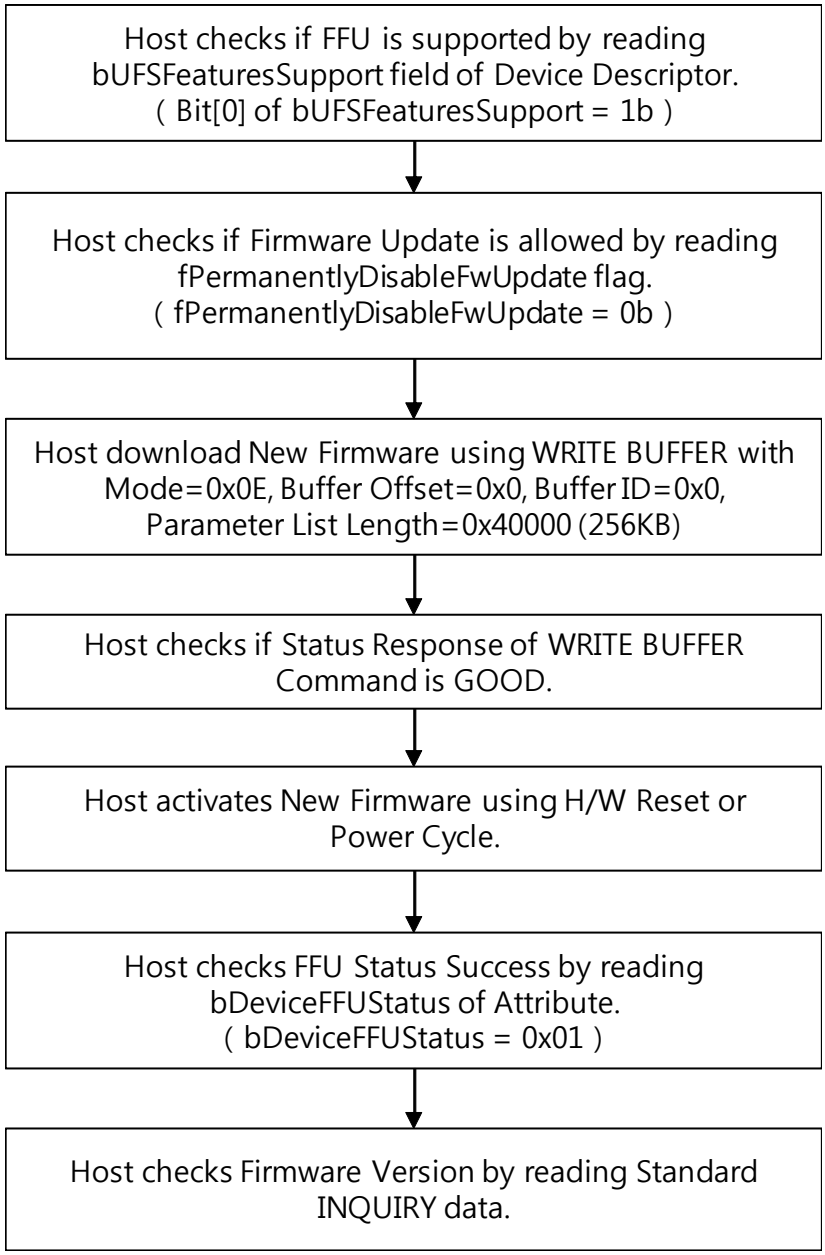
[Figure 5] Example of UFS Device Memory Organization

LU	Supported Size
BOOT LU	4MB ~ 256MB
RPMB LU	16MB

4. UFS Feature Notes

4.1 Field Firmware Update (FFU)

SK hynix supports microcode download based on Field Firmware Update using WRITE BUFFER command. For more details, see as the following chart like given below.



[Figure 6] FFU Flow chart

4.1.1 WRITE BUFFER Command Parameters

WRITE BUFFER Command Parameters				
Byte	**Bit**	**Parameters**	**Value**	**Remark**
0	7:0	Opcode	3Bh	
1	4:0	Mode	0Eh	Field Firmware Update
2	7:0	Buffer ID	00h	Buffer 0 supported
3:5	7:0	Buffer Offset	000000h	Buffer 0 byte offset
6:8	7:0	Parameter List Length	040000h	F/W binary size in bytes (256KB)
9	7:0	Control	00h	

4.1.2 FFU related Fields of Device Descriptor

FFU related Fields of Device Descriptor				
Offset	**Size**	**Field Name**	**MDV**	**Remark**
0x1F	1	bUFSFeaturesSupport	01h	FFU feature supported
0x20	1	bFFUTimeout	03h	Max FFU Timeout : 3 sec

4.1.3 FFU related Fields of Device Descriptor

FFU related Attribute				
IDN	**Size**	**Parameters**	**Access Property**	**Remark**
0x14	1	bDeviceFFUStatus	Read Only	Device FFU Status 00h: No information 01h: Successful microcode update 02h: Microcode corruption error 03h: Internal error 04h: Microcode version mismatch 05h-FEh: Reserved FFh: General Error

4.2 Supported VPD Pages

SK hynix supports VPD pages like below table.

EVPD	Page Code	VPD Page Name
0	00h	Standard INQUIRY data
1	00h	Supported VPD Pages
1	80h	Unit Serial Number
1	83h	Device Identification
1	86h	Extended INQUIRY Data
1	87h	Mode Page Policy
1	B0h	Block Limits VPD Page
1	B1h	Block Device Characteristics VPD Page
1	B2h	Logical Block Provisioning VPD page

4.3 Mode Pages

SK hynix supports UFS supported pages and subpage is not supported.

Page Code	Page Code	SUBPage Code	Page Name	Support
00h	00h	-	Vendor specific	Not Support
01h ~ 1Fh (SCSI Specific)	0Ah	00h (Device specific STANDARD page)	CONTROL	Support
	01h		READ-WRITE ERROR RECOVERY	Support
	08h		CACHING	Support
	-	01h~DFh	Device Specific SUBPAGE	Not Support
	-	E0h~FEh	Vendor Specific SUBPAGE	Not Support
	-	FFh	ALL SUBPAGES	Not Support
20h ~ 3Eh (Vendor Specific)	-	00h	Vendor Specific STANDARD	Not Support
	-	01h~FEh	Vendor Specific SUBPAGE	Not Support
	-	FFh	ALL SUBPAGES	Not Support
Return ALL pages	3Fh	00h	ALL PAGES	Support
	3Fh	01h~FEh	Reserved	Reserved
	3Fh	FFh	ALL SUBPAGES	Support

5. UFS General Parameters

5.1 Power Supplies

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage (memory)	V_{cc}	2.7	3.6	V	
Supply Voltage (controller and IO)	V_{ccq}	1.1	1.3	V	Not Used
Supply Voltage (secondary for controller and IO)	V_{ccq2}	1.70	1.95	V	
Supply power-up for 3.3V	tPRUH		35	ms	
Supply power-up for 1.8V	tPRUL		25	ms	
Supply power-up for 1.2V	tPRUV		20	ms	Not Used

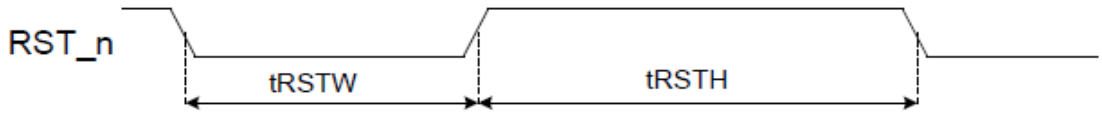
5.2 Reset Signal

5.2.1 Reset Signal Electrical Parameters

Parameter	Symbol	Min	Max	Unit	Remark
Input HIGH voltage	V_{IH}	0.65 * VCCQ	1.98	V	
Input LOW voltage	V_{IL}	VSS - 0.3	0.35 * VCCQ	V	

5.2.2 Reset Timing Parameters

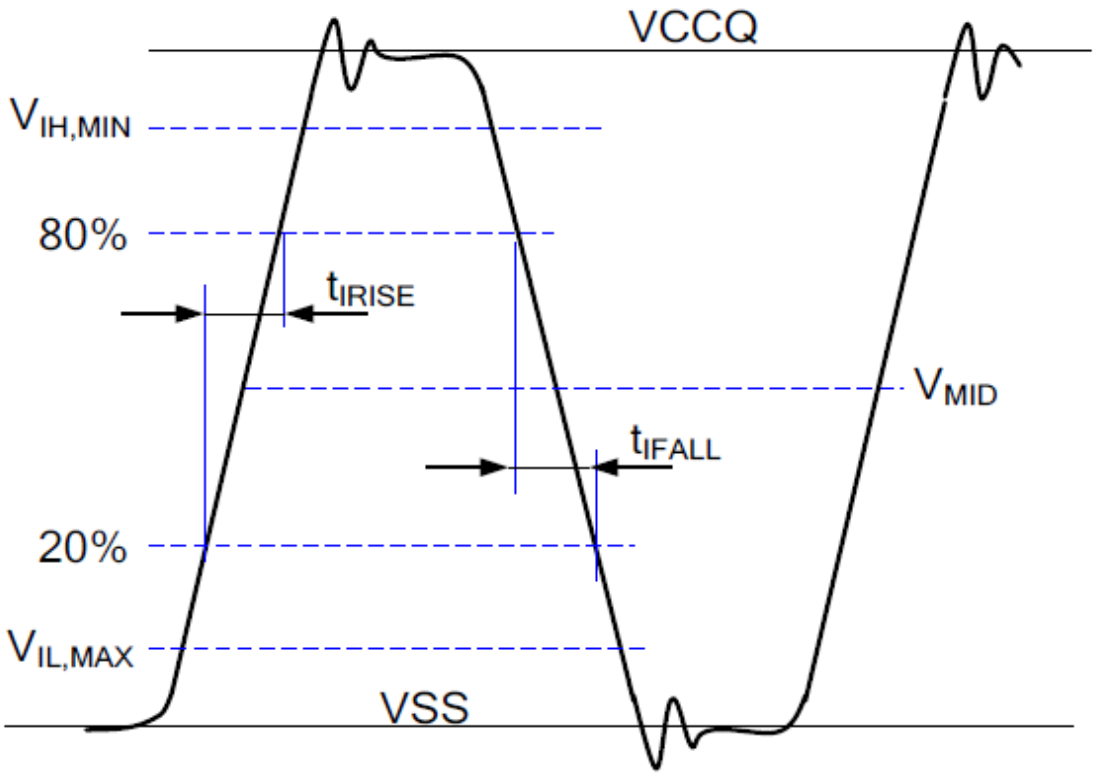
Symbol	Min	Max	Unit	Description
tRSTW	1	-	µs	RST_n Pulse Width
tRSTH	1	-	µs	RST_n High Period (Interval)
tRSTF	100	-	ns	RST_n Filter



[Figure 7] Reset Timing

5.3 Reference Clock

The M-PHY specification defines the reference clock optional for the State Machine Type I [MIPI M-PHY].



[Figure 8] Clock Input Levels, Rise Time, and Fall Time

Parameter	Symbol	Min	Max	Unit	Remark
Frequency	f_{ref}	19.2 **26 (Default)** 38.4 52		MHz	1
Frequency Error	f_{ERROR}	-150	+150	ppm	
Input High Voltage	V_{IH}	0.65 * VCCQ	1.8	V	2
Input Low Voltage	V_{IL}	0	0.35 * VCCQ	V	2
Input Clock Rise Time	t_{IRISE}	0.5	2	ns	3
Input Clock Fall Time	t_{IFALL}	0.5	2	ns	3
Duty Cycle	t_{DC}	45	55	%	4
Phase Noise	N	-	-66	dBC	5
Noise Floor Density (REFCLK Noise floor density from 50KHz to 10MHz)	$N_{Density}$	-	-140	dBC/Hz	6
Input Impedance	RL_{RX}	100		kΩ	7
	CL_{RX}	5		pF	
Input Leakage Current	I_{LKG}	-	10	μA	

- HS-BURST rates A and B are achieved with integer multipliers of f_{ref}.
- Figure 8 shows the input levels V_{IL},MAX to V_{IH},MIN.
- Clock rise time and clock fall time shall be measured from 20% to 80% of the window defined by V_{IL},MAX to V_{IH},MIN
- Clock duty cycle shall be measured at the Crossing of the REF_CLK signal with the midpoint VMID, defined as: VMID = (V_{IL},MAX + V_{IH},MIN) / 2
- Integrated single side band phase noise from 50KHZ to 10MHz. This parameter refers to the random jitter only.
- White noise floor. This parameter refers to the random jitter only.
- RL_{RX} and CL_{RX} include Rx package and Rx input impedance.

5.4 Bus Signal Levels

5.4.1 Output Level

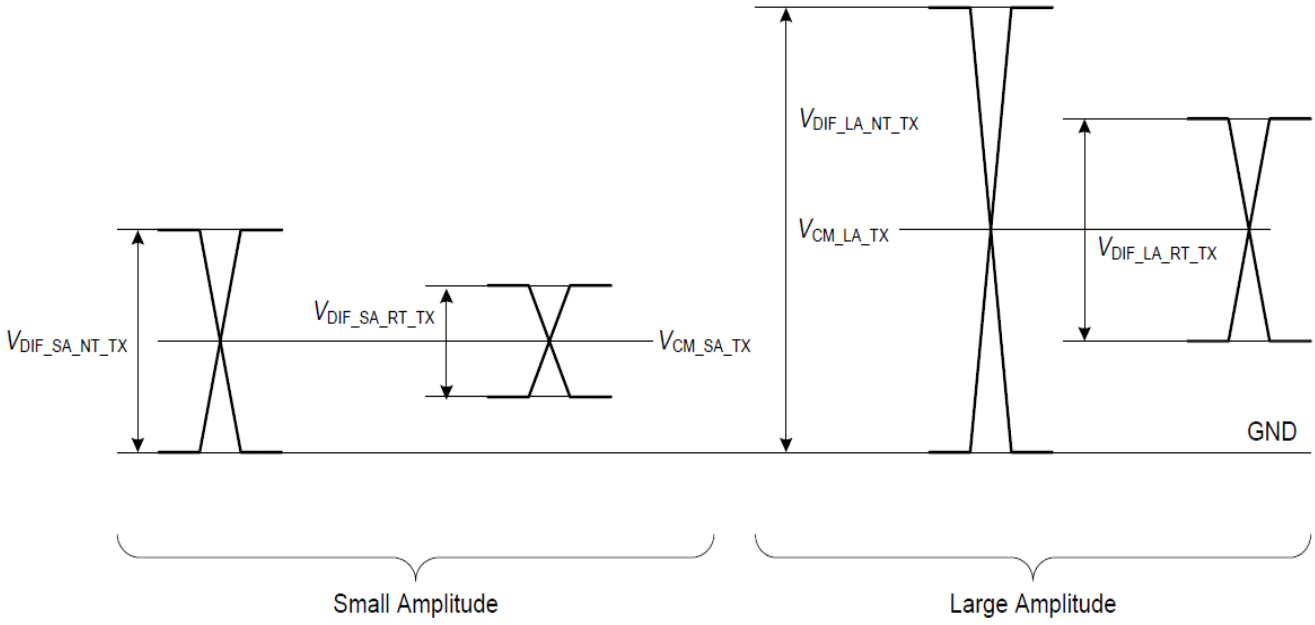
SK hynix UFS supports two different amplitudes.
1) the Large Amplitude (LA)
2) the Small Amplitude (SA)

Every M-TX in every LINK will start communication with LA after power up or reset.
Option to switch to SA mode shall be supported via a Configuration Attribute.

DOUT_t / DOUT_c pair should satisfy VCM_TX

$$V_{CM_TX}(t) = \frac{V_{TXDP}(t) + V_{TXDN}(t)}{2}$$

V_{TXDP} / V_{TXDN} = Positive / Negative Signal Voltage



[Figure 9] M-TX Signal Levels

5.4.1.1 Common M-TX Parameters

Symbol	Min	Max	Unit	Description
VDIF_DC_LA_RT_TX	160	240	mV	Large Amplitude differential TX DC voltage when the M-TX is terminated
VDIF_AC_LA_RT_TX	140	250	mV	Large Amplitude differential TX AC voltage when the M-TX is terminated
VDIF_DC_LA_NT_TX	320	480	mV	Large Amplitude differential TX DC voltage when the M-TX is NOT terminated
VDIF_AC_LA_NT_TX	280	500	mV	Large Amplitude differential TX AC voltage when the M-TX is NOT terminated
VDIF_DC_SA_RT_TX	100	130	mV	Small Amplitude differential TX DC voltage when the M-TX is terminated
VDIF_AC_SA_RT_TX	80	140	mV	Small Amplitude differential TX AC voltage when the M-TX is terminated
VDIF_DC_SA_NT_TX	200	260	mV	Small Amplitude differential TX DC voltage when the M-TX is NOT terminated
VDIF_AC_SA_NT_TX	160	280	mV	Small Amplitude differential TX AC voltage when the M-TX is NOT terminated
VCM_LA_TX	160	260	mV	Large Amplitude common-mode TX Voltage
VCM_SA_TX	80	190	mV	Small Amplitude common-mode TX Voltage
RSE_TX	40	60	Ω	Single-ended Output Resistance
RSE_PO_TX	-	10	KΩ	Single-ended Output Resistance in Stall or Sleep States

5.4.2 Input Level

DIN_t / DIN_c pair should satisfy VCM_RX.

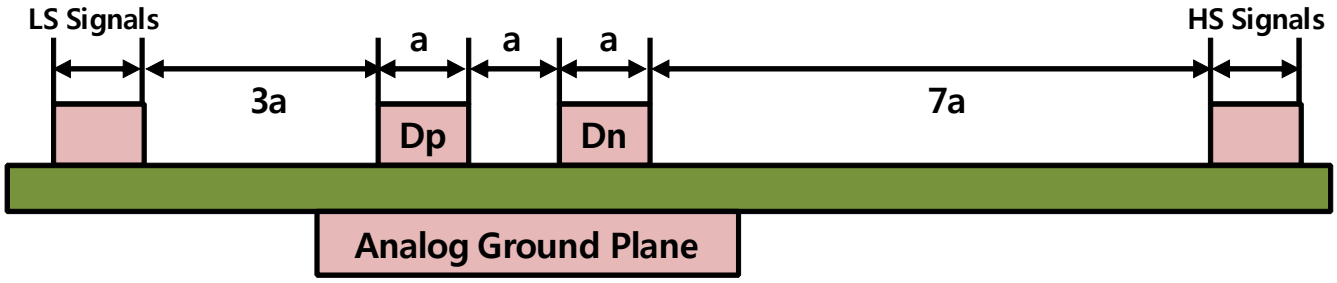
$$V_{CM_RX}(t) = \frac{V_{RXDP}(t) + V_{RXDN}(t)}{2}$$

Symbol	Min	Max	Unit	Description
VDIF_RT_RX	60	245	mV	Large Amplitude differential TX DC voltage when the M-TX is terminated
VDIF_NT_RX	120	490	mV	Large Amplitude differential TX AC voltage when the M-TX is terminated
VCM_RX	25	330	mV	Large Amplitude differential TX DC voltage when the M-TX is NOT terminated
RDIF_RX	80	110	Ω	Large Amplitude differential TX AC voltage when the M-TX is NOT terminated

5.5 PCB Guideline

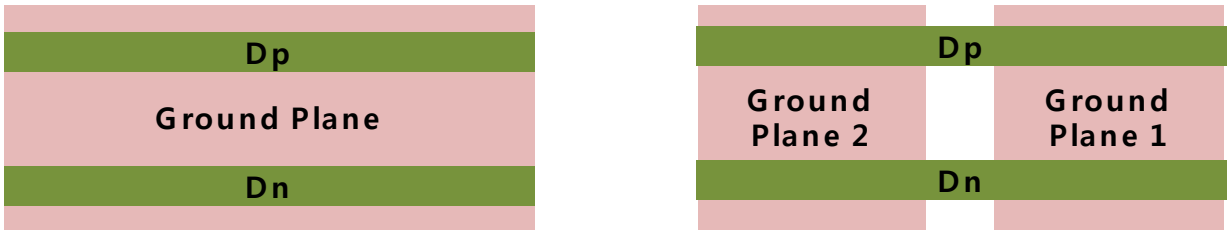
SK hynix recommends that you maintain the TX/RX differential pars (Dp/Dn) with 100Ω differential impedance through the range of operating frequencies and routed on the top layer without any vias. This ensures minimum reflections and signal integrity degradation at the higher rates.
Calculate the trace width and spacing for specific PCB characteristics such as copper weight, dielectric thickness, and so on. Route as a differential pair with matching lengths.

To minimize the crosstalk, take care of signal traces which are routed close to the TX/RX data differential pairs. The minimum recommended spacing is 3x for low-speed non-periodic signals and 7x for high-speed periodic signals. A continuous ground plane below the Dp/Dn lines is required.



[Figure 10] Crosstalk Protection for Dp/Dn Lines

With the high-speed signals routed on the top layer, there must be a ground plane immediately below these lines (microstrip line configuration). Also, this should be unique in order to avoid crossing between different ground planes



[Figure 11] PCB Differential Traces

6. Latency Time

Timing Parameter	Value	Remark
Read	Max 100ms	
Write	Max 200ms	
SYNC CACHE	Max 300ms	
Urgent BKOP	Max 55sec	
Discard (1G)	Max 750ms	* 1G discard condition
Format (Wipe)	32GB, 64GB : Max 60 sec 128GB : Max 90 sec	
Purge	Max 1 min	

- File system overhead is not considered
- Not 100% tested but tested with worst corner.

7. UPIU Transaction Codes

SK hynix UFS supports following UPIU transaction codes. Each command is used with corresponding UPIU. It is not allowed to use undefined codes. Refer to UFS specification for more detail information.

Initiator To Target	Transaction Code	Target to Initiator	Transaction Code
NOP Out	00 0000b	NOP In	10 0000b
Command	00 0001b	Response	10 0001b
Data Out	00 0010b	Data In	10 0010b
Task Management Request	00 0100b	Task Management Response	10 0100b
Reserved	01 1001b	Ready To Transfer	11 0001b
Query Request	01 0110b	Query Response	11 0110b
Reserved	01 1111b	Reject UPIU	11 1111b
Reserved	Others	Reserved	Others

7.1 UFS SCSI Command

Command name	Opcode	Command name	Opcode
FORMAT UNIT	04h	SECURITY PROTOCOL IN	A2h
INQUIRY	12h	SECURITY PROTOCOL OUT	B5h
MODE SELECT (10)	55h	SEND DIAGNOSTIC	1Dh
MODE SENSE (10)	5Ah	START STOP UNIT	1Bh
PRE-FETCH (10)	34h	SYNCHRONIZE CACHE (10)	35h
PRE-FETCH (16)	90h	SYNCHRONIZE CACHE (16)	91h
READ (6)	08h	TEST UNIT READY	00h
READ (10)	28h	UNMAP	42h
READ (16)	88h	VERIFY (10)	2Fh
READ BUFFER	3Ch	WRITE (6)	0Ah
READ CAPACITY (10)	25h	WRITE (10)	2Ah
READ CAPACITY (16)	9Eh	WRITE (16)	8Ah
REPORT LUNS	A0h	WRITE BUFFER	3Bh
REQUEST SENSE	03h		

8. UFS Descriptors, Flags, Attributes

The UFS modules support following UFS descriptors defined in UFS specification. Refer to UFS specification for more detail information

DESCRIPTOR TYPE	DESCRIPTOR IDN	DESCRIPTOR TYPE	DESCRIPTOR IDN
DEVICE	00h	RFU	06h
CONFIGURATION	01h	GEOMETRY	07h
UNIT	02h	POWER	08h
RFU	03h	DEVICE HEALTH	09h
INTERCONNECT	04h	RFU	0Ah~FFh
STRING	05h		

8.1 Device Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	40h	Size of Device Descriptor
01h	1	bDescriptorIDN	00h	Device Descriptor Type Identifier
02h	1	bDevice	00h	00h: Device
03h	1	bDeviceClass	00h	00h: Mass Storage
04h	1	bDeviceSubClass	00h	00h: Embedded Bootable
05h	1	bProtocol	00h	00h: SCSI
06h	1	bNumberLU	User Conf.	Number of Logical Units (Default: 00h)
07h	1	bNumberWLU	04h	04h: 4 Well known logical units exist
08h	1	bBootEnable	User Conf.	00h: Boot feature disabled (Default) 01h: Bootable feature enabled
09h	1	bDescrAccessEn	User Conf.	00h: Device Descriptor access disabled (Default) 01h: Device Descriptor access enabled
0Ah	1	bInitPowerMode	User Conf.	00h: UFS-Sleep Mode 01h: Active Mode (Default)
0Bh	1	bHighPriorityLUN	User Conf.	00h-07h: Configured LUN has high priority 7Fh: All logical units have the same priority (Default)
0Ch	1	bSecureRemovalType	User Conf.	00h: Information removed by an erase of the physical memory (Default) 01h: Information removed by overwriting the addressed locations with a single character followed by an erase 02h: Information removed by overwriting the addressed locations with a character, its complement, then a random character 03h: Information removed using a vendor define mechanism
0Dh	1	bSecurityLU	01h	01h: RPMB
0Eh	1	bBackgroundOpsTermLat	FFh	bBackgroundOpsTermLat defines the maximum latency for the termination of ongoing background operations. The latency is expressed in units of 10ms.
0Fh	1	bInitActiveICCLevel	User Conf.	bInitActiveICCLevel defines the bActiveICCLevel value after power on or reset Valid range: 00h to 0Fh. (Default 00h)
10h	2	wSpecVersion	0210h	Specification version 2.10
12h	2	wManufactureDate	Device Specific	Manufacturing Date ex) 0515h = May 2015

OFFSET	SIZE	NAME	VALUE	Description
14h	1	iManufacturerName	01h	Index to Manufacturer Name String
15h	1	iProductName	02h	Index to Product Name String
16h	1	iSerialNumber	03h	Index to Serial Number String
17h	1	iOemID	04h	Index to OEM ID String
18h	2	wManufacturerID	1ADh	Manufacturer ID
1Ah	1	bUD0BaseOffset	10h	Unit Descriptor 0 Base Offset
1Bh	1	bUDConfigPLength	10h	Unit Descr. Config. Param. Length Total size of the configurable Unit Descriptor parameters
1Ch	1	bDeviceRTTCap	02h	RTT Capability of device Maximum number of outstanding RTTs supported by device
1Dh	2	wPeriodicRTCUpdate	User Conf.	Frequency and method of Real-Time Clock update (Default 000h)
1Fh	1	bUFSFeatureSupport	01h	01h: Field Firmware Update (FFU) supported
20h	1	bFFUTimeout	03h	Field Firmware Update Timeout. The maximum time is expressed in units of seconds.
21h	1	bQueueDepth	00h	0: The device implements the per-LU queueing architecture.
22h	2	wDeviceVersion	TBD	Device version
24h	1	bNumSecureWPArea	20h	Number of Secure Write Protect Areas
25h	4	dPSAMaxDataSize	00h	PSA Maximum Data Size
29h	1	bPSAStateTimeout	00h	PSA State Timeout
2Ah	1	iProductRevisionLevel	05h	Index to the string which contains the Product Revision Level
2Bh	5	Reserved	00h	Reserved
21h	16	Reserved	00h	Reserved for Unified Memory Extension standard

8.2 Geometry Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	48h	Size of Geometry Descriptor
01h	1	bDescriptorIDN	07h	Geometry Descriptor Type Identifier
02h	1	bMediaTechnology	00h	Resrved
03h	1	Resrved	00h	Resrved
04h	8	qTotalRawDeviceCapacity	3B9E000h (32GB) 7734000h (64GB) EE60000h (128GB)	Total Raw Device Capacity Total memory quantity available to the user to configure the device logical units (RPMB excluded) It is expressed in units of 512 Bytes.
0Ch	1	bMaxNumberLU	00h	00h: 8 Logical Units
0Dh	4	dSegmentSize	00002000h	Segment Size It is expressed in units of 512 Bytes
11h	1	bAllocationUnitSize	01h	Allocation Unit Size Value expressed in number of Segments
12h	1	bMinAddrBlockSize	08h	Minimum addressable block size (4KB) Value expressed in unit of 512 Bytes
13h	1	bOptimalReadBlockSize	80h	Optimal read block size (64KB) Value expressed in unit of 512 Bytes
14h	1	bOptimalWriteBlockSize	80h	Optimal write block size (64KB) Value expressed in unit of 512 Bytes
15h	1	bMaxInBufferSize	40h	Max data-in buffer size (32KB) Value expressed in unit of 512 Bytes
16h	1	bMaxOutBufferSize	40h	Max data-out buffer size (32KB) Value expressed in unit of 512 Bytes
17h	1	bRPMB_ReadWriteSize	20h	Maximum number of RPMB frames (256 byte of data) allowed in Security Protocol In and Security Protocol Out.
18h	1	bDynamicCapacity ResourcePolicy	00h	00h: Spare blocks resource management policy is per logical unit. The host should release amount of logical blocks from each logical unit as asked by the device.
19h	1	bDataOrdering	00h	00h: out-of-order data transfer is not supported by the device. 01h: out-of-order data transfer is supported by the device.
1Ah	1	bMaxContexIDNumber	0Fh	Maximum available number of contexts which are supported by the device.
1Bh	1	bSysDataTagUnitSize	00h	bSysDataUnitSize provides system data tag unit size, which can be calculated as in the following. (in bytes) Tag Unit Size = $2^{bSysDataTagUnitSize}$ x bMinAddrBlockSize x 512

OFFSET	SIZE	NAME	VALUE	Description
1Ch	1	bSysDataTagResSize	00h	This field is defined to inform the host about the maximum storage area size in bytes allocated by the device to handle system data by the tagging mechanism. System Data Tag Resource Size = Tag Unit Size x floor($\frac{qTotalRawDeviceCapacity \times 2^{bSysDataTagResSize-1}}{Tag\ Unit\ Size}$) The range of valid bSysDataTagResSize values is from 0h to 6h Values in range of 7h to 0xFF are reserved. The formula covers a range from about 0.1% to 6.25% of the device capacity.
1Dh	1	bSupportedSecRTypes	09h	Supported Secure Removal Types Bit map which represents the supported Secure Removal types. Bit 0: Information removed by an erase of the physical memory Bit 1: Information removed by overwriting the addressed locations with a single character followed by an erase Bit 2: Information removed by overwriting the addressed locations with a character, its complement, then a random character Bit 3: Information removed using a vendor define mechanism Others: Reserved A value of one means that the corresponding Secure Removal type is supported.
1Eh	2	wSupportedMemory Types	8079h	Bit 0: Normal memory type Bit 1: System code memory type Bit 2: Non-Persistent memory type Bit 3: Enhanced memory type 1 Bit 4: Enhanced memory type 2 Bit 5: Enhanced memory type 3 Bit 6: Enhanced memory type 4 Bit 15: RPMB memory type * SK hynix supports SLC type for all enhanced memory type. This device has no difference of each enhanced type.
20h	4	dSystemCodeMaxNAllocU	00000000h	System code memory type is not supported.
24h	2	wSystemCodeCapAdjFac	0000h	System code memory type is not supported.
26h	4	dNonPersistMaxNAllocU	00000000h	Non-Persistent memory type is not supported.
2Ah	2	wNonPersistCapAdjFac	0000h	Non-Persistent memory type is not supported.
2Ch	4	dEnhanced1MaxNAllocU	1DCFh (32GB) 3B9Ah (64GB) 7730h (128GB)	Max Number of Allocation Units for the Enhanced memory type 1

OFFSET	SIZE	NAME	VALUE	Description
30h	2	wEnhanced1CapAdjFac	0200h	Capacity Adjustment Factor for the Enhanced memory type 1 Factor used to adjust the memory capacity of this memory property from normal memory: Capacity Enhanced1 = CapacityNormalMem / CapAdjFac wEnhanced1CapAdjFac = INTEGER(256 × CapAdjFac)
32h	4	dEnhanced2MaxNAllocU	1DCFh (32GB) 3B9Ah (64GB) 7730h (128GB)	Enhanced memory type 2 is not supported.
36h	2	wEnhanced2CapAdjFac	0200h	Enhanced memory type 2 is not supported.
38h	4	dEnhanced3MaxNAllocU	1DCFh (32GB) 3B9Ah (64GB) 7730h (128GB)	Enhanced memory type 3 is not supported.
3Ch	2	wEnhanced3CapAdjFac	0200h	Enhanced memory type 3 is not supported.
3Eh	4	dEnhanced4MaxNAllocU	1DCFh (32GB) 3B9Ah (64GB) 7730h (128GB)	Enhanced memory type 4 is not supported.
42h	2	wEnhanced4CapAdjFac	0200h	Enhanced memory type 4 is not supported.
44h	4	dOptimalLogicalBlockSize	0h	Optimal Logical Block Size Bit [3:0]: Normal memory type Bit [7:4]: System code memory type Bit [11:8]: Non-Persistent memory type Bit [15:12]: Enhanced memory type 1 Bit [19:16]: Enhanced memory type 2 Bit [23:20]: Enhanced memory type 3 Bit [27:24]: Enhanced memory type 4 Bit [31:28]: Reserved The optimal logical block size for each memory type can be caculated from the related dOptimalLogicalBlockSize field as indicated in the following: Optimal Logical Block Size = 2^(dOptimalLogicalBlockSize field)x bMinAddrBlockSize x 512byte

8.3 Unit Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	23h	Size of Unit Descriptor
01h	1	bDescriptorIDN	02h	UNIT Descriptor Type Identifier
02h	1	bUnitIndex	00h~07h	Unit Index
03h	1	bLUEnable	User Conf.	Logical Unit Enable 00h: Logical Unit disabled (Default) 01h: Logical Unit enabled Others: Reserved
04h	1	bBootLunID	User Conf.	Boot LUN ID 00h: Not bootable (Default) 01h: Boot LU A 02h: Boot LU B Others: Reserved
05h	1	bLUWriteProtect	User Conf.	Logical Unit Write Protect 00h: LU not write protected (Default) 01h: LU write protected when fPowerOnWPEn = 1 02h: LU permanently write protected when fPermanentWPEn = 1 Others: Reserved
06h	1	bLUQueueDepth	00h	Logical Unit Queue Depth Queue depth available in this LU Queue depth of '0' means best effort by device to service the command task.
07h	1	bPSASensitive	00h	00h: LU is not sensitive to soldering. 01h: LU is sensitive to soldering. Others: Reserved
08h	1	bMemoryType	User Conf.	Memory Type bMemoryType defines logical unit memory type. 00h: Normal Memory (Default) 01h: System code memory type (Not supported) 02h: Non-Persistent memory type (Not supported) 03h: Enhanced memory type 1 04h: Enhanced memory type 2 (Not supported) 05h: Enhanced memory type 3 (Not supported) 06h: Enhanced memory type 4 (Not supported) Others: Reserved

OFFSET	SIZE	NAME	VALUE	Description
09h	1	bDataReliability	User Conf.	Data Reliability bDataReliability defines the device behavior when a power failure occurs during a write operation to the logical unit. 00h: the logical unit is not protected. Logical unit's entire data might be lost as a result of a power failure during a write operation. (Default) 01h: logical unit is protected. Logical unit's data is protected against power failure. Others: Reserved
0Ah	1	bLogicalBlockSize	User conf.	Logical Block Size (Default 4KB) The size of addressable logical blocks is equal the result of exponentiation with as base the number two and as exponent the bLogicalBlockSize value: $2^{bLogicalBlockSize}$(i.e., bLogicalBlockSize = 0Ch corresponds to 4 KByte Logical Block Size). Its minimum value is 0Ch, which corresponds to 4 Kbyte.
0Bh	8	qLogicalBlockCount	User conf.	Logical Block Count (Default 00h) Total number of addressable Logical Blocks in the LU in Logical Block Size unit qLogicalBlockCount can be configured setting the dNumAllocUnits parameter of the Configuration Descriptor.
13h	4	dEraseBlockSize	00000001h	Erase Block Size (4KB) in number of Logical Blocks dEraseBlockSize value is updated automatically by the device after device configuration.
17h	1	bProvisioningType	0x00h	Provisioning Type 00h: Thin Provisioning is disabled (default) 02h: Thin Provisioning is enabled and TPRZ = 0 03h: Thin Provisioning is enabled and TPRZ = 1 Others: Reserved
18h:1Fh	8	qPhyMemResourceCount	0000000000000000h	Physical Memory Resource Count Total physical memory resource available in the logical unit. Value expressed in units of Logical Block Size.
20h	2	wContextCapabilities	0000h	Default 0000h Bit [3:0]: MaxContextID is the maximum amount of contexts that the LU supports simultaneously. The sum of all MaXContextID must not exceed bMaxContexIDNumber. Bit [6:4]: LARGE_UNIT_MAX_MULTIPLIER_M1 is the highest multiplier that can be configured for Large Unit contexts, minus one. Large Unit contexts may be configured to have a multiplier in the range: 1 ≤ multiplier ≤(LARGE_UNIT_MAX_MULTIPLIER_M1 + 1) This field is read only. Bit [15:7]: Reserved
22h	1	bLargeUnitGranularity_M1	00h	Large Unit is not supported.

8.3.1 RPMB Unit Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	23h	Size of RPMB Unit Descriptor
01h	1	bDescriptorIDN	02h	RPMB Unit Descriptor Type Identifier
02h	1	bUnitIndex	C4h	Unit Index
03h	1	bLUEnable	01h	01h: Logical Unit enabled
04h	1	bBootLunID	00h	00h: Not bootable
05h	1	bLUWriteProtect	00h	00h: LU not write protected
06h	1	bLUQueueDepth	01h	Queue depth available in this LU
07h	1	bPSASensitive	00h	
08h	1	bMemoryType	0Fh	0Fh: RPMB Memory Type
09h	1	Reserved	00h	
0Ah	1	bLogicalBlockSize	08h	The size of addressable logical blocks is equal the result of exponentiation with as base the number two and as exponent the bLogicalBlockSize value: 2bLogicalBlockSize (i.e., bLogicalBlockSize = 08h corresponds to 256 Byte Logical Block Size)
0Bh	8	qLogicalBlockCount	00010000h	Total number of addressable Logical Blocks of the RPMB LU in Logical Block Size unit. For RPMB, Logical Block Count shall be a multiple of 512. (i.e., 128 KByte)
13h	4	dEraseBlockSize	00h	In number of Logical Blocks. For RPMB, Erase Block Size is ignored; set to '0'
17h	1	pProvisioningType	00h	00h:Thin Provisioning is disabled.
18h:1Fh	8	pPhyMemResourceCount	00010000h	Total physical memory resource available in the logical unit. Value expressed in units of bLogicalBlockSize The dynamic device capacity feature does not apply to the RPMB well known logical unit. Therefore qPhyMemResourceCount value is always equal to qLogicalBlockCount value.
20h:22h	3	Reserved	000000h	

8.4 Power Parameters Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	62h	Size of this descriptor
01h	1	bDescriptorIDN	08h	Power Parameters Descriptor Type Identifier
02h	2	wActiveICCLevelsVCC(0)	32GB 8118h 64GB 8118h 128GB 812Ch	2 byte maximum VCC current value for each of the 16 active current consumption levels starting with level 0
04h	2	wActiveICCLevelsVCC(1)		
06h	2	wActiveICCLevelsVCC(2)		
08h	2	wActiveICCLevelsVCC(3)		
0Ah	2	wActiveICCLevelsVCC(4)		
0Ch	2	wActiveICCLevelsVCC(5)		
0Eh	2	wActiveICCLevelsVCC(6)		
10h	2	wActiveICCLevelsVCC(7)		
12h	2	wActiveICCLevelsVCC(8)		
14h	2	wActiveICCLevelsVCC(9)		
16h	2	wActiveICCLevelsVCC(10)		
18h	2	wActiveICCLevelsVCC(11)		
1Ah	2	wActiveICCLevelsVCC(12)		
1Ch	2	wActiveICCLevelsVCC(13)		
1Eh	2	wActiveICCLevelsVCC(14)		
20h	2	wActiveICCLevelsVCC(15)		
22h	2	wActiveICCLevelsVCCQ(0)	0000h	Not Used
24h	2	wActiveICCLevelsVCCQ(1)	0000h	Not Used
26h	2	wActiveICCLevelsVCCQ(2)	0000h	Not Used
28h	2	wActiveICCLevelsVCCQ(3)	0000h	Not Used
2Ah	2	wActiveICCLevelsVCCQ(4)	0000h	Not Used
2Ch	2	wActiveICCLevelsVCCQ(5)	0000h	Not Used
2Eh	2	wActiveICCLevelsVCCQ(6)	0000h	Not Used
30h	2	wActiveICCLevelsVCCQ(7)	0000h	Not Used
32h	2	wActiveICCLevelsVCCQ(8)	0000h	Not Used
34h	2	wActiveICCLevelsVCCQ(9)	0000h	Not Used

OFFSET	SIZE	NAME	VALUE	Description
36h	2	wActiveICCLevelsVCCQ(10)	0000h	Not Used
38h	2	wActiveICCLevelsVCCQ(11)	0000h	Not Used
3Ah	2	wActiveICCLevelsVCCQ(12)	0000h	Not Used
3Ch	2	wActiveICCLevelsVCCQ(13)	0000h	Not Used
3Eh	2	wActiveICCLevelsVCCQ(14)	0000h	Not Used
40h	2	wActiveICCLevelsVCCQ(15)	0000h	Not Used
42h	2	wActiveICCLevelsVCCQ2(0)	32GB 81F4h 64GB 81F4h 128GB 8224h	2 byte maximum VCCQ2 current value for each of the 16 active current consumption levels starting with level 0
44h	2	wActiveICCLevelsVCCQ2(1)		
46h	2	wActiveICCLevelsVCCQ2(2)		
48h	2	wActiveICCLevelsVCCQ2(3)		
4Ah	2	wActiveICCLevelsVCCQ2(4)		
4Ch	2	wActiveICCLevelsVCCQ2(5)		
4Eh	2	wActiveICCLevelsVCCQ2(6)		
50h	2	wActiveICCLevelsVCCQ2(7)		
52h	2	wActiveICCLevelsVCCQ2(8)		
54h	2	wActiveICCLevelsVCCQ2(9)		
56h	2	wActiveICCLevelsVCCQ2(10)		
58h	2	wActiveICCLevelsVCCQ2(11)		
5Ah	2	wActiveICCLevelsVCCQ2(12)		
5Ch	2	wActiveICCLevelsVCCQ2(13)		
5Eh	2	wActiveICCLevelsVCCQ2(14)		
60h	2	wActiveICCLevelsVCCQ2(15)		

8.5 Interconnect Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	06h	Size of Interconnect Descriptor
01h	1	bDescriptorIDN	04h	Interconnect Description Type Identifier
02h	2	bcdUniproVersion	0160h	MIPI UniPro version number in BCD format (i.e., version 1.60 = 0160h)
04h	2	bcdMphyVersion	0300h	MIPI M-PHY version number in BCD format (i.e., version 3.00 = 0300h)

8.6 Manufacturer Name String Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	12h	Size of String Descriptor
01h	1	bDescriptorIDN	05h	String Descriptor Type Identifier
02h	2	UC[0]	0053h	Unicode string character ("S")
04h	2	UC[1]	004Bh	Unicode string character ("K")
06h	2	UC[2]	0048h	Unicode string character ("H")
08h	2	UC[3]	0059h	Unicode string character ("Y")
0Ah	2	UC[4]	004Eh	Unicode string character ("N")
0Ch	2	UC[5]	0049h	Unicode string character ("I")
0Eh	2	UC[6]	0058h	Unicode string character ("X")
10h	2	UC[7]	0000h	"NULL"

8.7 Product Name String Descriptor

OFFSET	SIZE	NAME	32GB	64GB	128GB	Description
00h	1	bLength	22h	22h	22h	Size of String Descriptor
01h	1	bDescriptorIDN	05h	05h	05h	Type Identifier
02h	2	UC[0]	68h	68h	68h	
04h	2	UC[1]	42h	43h	44h	
06h	2	UC[2]	38h	38h	38h	
08h	2	UC[3]	61h	61h	61h	
0Ah	2	UC[4]	4Ch	4Ch	4Ch	
0Ch	2	UC[5]	31h	31h	31h	
0Eh~	10	UC[6]~UC[15]	0000h	0000h	0000h	"NULL"

8.8 OEM ID String Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	0Ah	Size of String Descriptor
01h	1	bDescriptorIDN	05h	String Description Type Identifier
02h	2	UC[0]	0030h	
04h	2	UC[1]	0031h	
06h	2	UC[2]	0041h	
08h	2	UC[3]	0044h	

8.9 Serial Number String Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	0Eh	Size of String Descriptor
01h	1	bDescriptorIDN	05h	String Descriptor Type Identifier
02h	2	UC[0]	-	Unique serial number hex code
04h	2	UC[1]	-	Unique serial number hex code
06h	2	UC[2]	-	Unique serial number hex code
08h	6	UC[3]~UC[5]	0000h	"NULL"

SK hynix supports 6 Bytes serial Number which is assigned by unique hex-code at each device. If some part of them (less than 6 bytes) are used, it couldn't be guranteed uniqueness.

8.10 Product Revision Level String Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	0Ah	Size of String Descriptor
01h	1	bDescriptorIDN	05h	String Description Type Identifier
02h	2	UC[0]	45h	
04h	2	UC[1]	30h	
06h	2	UC[2]	30h	
08h	2	UC[3]	32h	

8.11 Device Health Descriptor

OFFSET	SIZE	NAME	VALUE	Description
00h	1	bLength	25h	Size of Device Health Descriptor
01h	1	bDescriptorIDN	09h	Device Health Descriptior Type Identifier
02h	1	bPreEOLInfo	Device Specific	Pre End of Life Information Thie field procvides indication about device life time reflected by average reserved blocks. 00h: Not defined 01h: Normal 02h: Warning Consumed 80% of reserved blocks 03h: Critical Consumed 90% of reserved blocks Others: Reserved
03h	1	bDeviceLifeTimeEstA	Device Specific	This field provieds an indication of the device life time based on the amount of performed program/erase cycels. The caculation method is vendor specific and reffered as method A. 00h: information not available 01h: 0%~10% device life time used 02h: 10%~20% device life time used 03h: 20%~30% device life time used 04h: 30%~40% device life time used 05h: 40%~50% device life time used 06h: 50%~60% device life time used 07h: 60%~70% device life time used 08h: 70%~80% device life time used 09h: 80%~90% device life time used 0Ah: 90%~100% device life time used 0Bh: Exceeded its maximum estimated device life time Others: Reserved

8.11 Device Health Descriptor (Continued)

OFFSET	SIZE	NAME	VALUE	Description
04h	1	bDeviceLifeTimeEstB	Device Specific	This field provieds an indication of the device life time based on the amount of performed program/erase cycels. The caculation method is vendor specific and reffered as method B. 00h: Information not available 01h: 0%~10% device life time used 02h: 10%~20% device life time used 03h: 20%~30% device life time used 04h: 30%~40% device life time used 05h: 40%~50% device life time used 06h: 50%~60% device life time used 07h: 60%~70% device life time used 08h: 70%~80% device life time used 09h: 80%~90% device life time used 0Ah: 90%~100% device life time used 0Bh: Exceeded its maximum estimated device life time Others: Reserved
05h	1	bFFUCount	Device Specific	Success count of FFU to higher (not same) version firmware
06h	2	wFactoryBadBlockCount	Device Specific	Initial bad block count
08h	2	wRuntimeBadBlockCount	Device Specific	Run time bad block count
0Ah	2	wMaxBlockEraseCount	Device Specific	Maximum NAND block erase count
0Ch	2	wMinBlockEraseCount	Device Specific	Minimum NAND block erase count
0Eh	2	wAveBlockEraseCount	Device Specific	Average NAND block erase coun
10h	2	wReadReclaimCount	Device Specific	Count number of read reclaim operation
12h	4	dSPOCount	Device Specific	Count number of Sudden power off. If count is FFFFFFFFh, it will not be increased further.
16h	4	dTotalWriteSize100M	Device Specific	Total write size. unit is 100MB.
1Ah	4	dLVDCount	Device Specific	Low Voltage Detection of VCC, VCCQ power supply. Bit [31:16]: LVD count of VCC(3.3V) Bit [15:0]: LVD count of VCCQ(1.8V)
1Eh	7	Reserved		

8.12 UFS Flags

IDN	NAME	TYPE	Default	Description
00h	Reserved		-	
01h	fDeviceInit	Read/ Set only	0	Device Initialization Host sets fDeviceInit flag to initiate device initialization after boot process is completed. Device resets flag when device initialization is completed. 0b: Device initialization completed or not started yet 1b: Device initialization in progress
02h	fPermanentWPEn	Read/ Write Once	0	Permanent Write Protection Enable fPermanentWPEn enables permanent writeprotection on all logical units configured as permanent protected; it cannot be toggled or cleared once it is set. 00h: Permanent write protection disabled 01h: Permanent write protection enabled
03h	fPowerOnWPEn	Read/ Power-on Reset	0	Power On Write Protection Enable fPowerOnWPEn enables the write protection on all logical units configured as power on write protected. If fPowerOnWPEn is equal to one and the device receive a Query Request to clear or toggle this flag, the Query Request shall fail and Response field shall be set to "F8h"(Parameter already written). The device shall set fPowerOnWPEn to zero in the event of power cycle or hardware reset. 0b: Power on write protection disabled 1b: Power on write protection enabled
04h	fBackgroundOpsEn	Read/ Volatile	1	Background Operations Enable 0b: Device is not permitted to run background operations. 1b: Device is permitted to run background operations.
05h	fDeviceLifeSpanModeEn	Read/ Volatile	0	Device Life Span Mode 0b: Device Life Span Mode is disabled. 1b: Device Life Span Mode is enabled.
06h	fPurgeEnable	Write Only/ Volatile	0	Purge Enable 0b: Purge operation is disabled. 1b: Purge operation is enabled. This flag shall only be set when the command queue of all logical units are empty and the bPurgeStatus is 00h (Idle). fPurgeEnable is automatically cleared by the UFS device when the operation completes or an error condition occurs. fPurgeEnable can be cleared by the host to interrupt an ongoing purge operation.
07h	Reserved		-	Reserved

IDN	NAME	TYPE	Default	Description
08h	fPhyResourceRemoval	Read/ Persistent	0	Physical Resource Removal The host sets this flag to one to indicate that the dynamic capacity operation shall commence upon device EndPointReset or hardware reset. The device shall reset this flag to zero after completion of dynamic capacity operation. The host cannot reset this flag.
09h	fBusyRTC	Read Only	0	Busy Real Time Clock 0b: Device is not executing internal operation related to RTC. 1b: Device is executing internal operation related to RTC. When this flag is set to one, it is recommended for the host to not send commands to the device.
0Ah	Reserved		-	Reserved
0Bh	fPermanentlyDisableFw Update	Read/ Write Once	0	Permanently Disable Firmware Update 0b: The UFS device firmware may be modified 1b: The UFS device shall permanently disallow future firmware updates to the UFS device

8.13 UFS Attributes

IDN	NAME	TYPE	Size [Byte]	MDV	Description
00h	bBootLunEn	Read/ Persistent	1	00h	Boot LUN Enable 00h: Boot disabled 01h: Enabled boot from Boot LU A 02h: Enabled boot from Boot LU B All others: Reserved When bBootLunEn = 00h the boot feature is disabled, the device behaves as if bBootEnable would be equal to 0
01h	Reserved		1	-	
02h	bCurrentPowerMode	Read Only	1	11h	Current Power Mode 00h: Idle mode 10h: Pre-Active mode 11h: Active mode 20h: Pre-Sleep mode 22h: UFS-Sleep mode 30h: Pre-Power Down mode 33h: UFS-Power Down mode Others: Reserved
03h	bActiveICCLevel	Read/ Persistent	1	00h	bActiveICCLevel defines the maximum current consumption allowed during Active Mode. 00h: Lowest Active ICC level 0Fh: Highest Active ICC level Others: Reserved Valid range : 00h to 0Fh.
04h	bOutOfOrderDataEn	Read/ Write Once	1	00h	Out of Order Data transfer Enable 00h: Out-of-order data transfer is disabled. 01h: Out-of-order data transfer is enabled. Others: Reserved This bit shall have effect only when bDataOrdering = 01h.
05h	bBackgroundOpStatus	Read Only	1	00h	Background Operations Status Device health status for background operation 00h: Not required 01h: Required, not critical 02h: Required, performance impact 03h: Critical Others: Reserved
06h	bPurgeStatus	Read Only	1	00h	Purge Operation Status 00h: Idle (purge operation disabled) 01h: Purge operation in progress 02h: Purge operation stopped prematurely 03h: Purge operation completed successfully 04h: Purge operation failed due to logical unit queue not empty 05h: Purge operation general failure When the bPurgeStatus is equal to the values 02h, 03h, 04h or 05h, the bPurgeStatus is automatically cleared to 00h (Idle) the first time that it is read.

IDN	NAME	TYPE	Size [Byte]	MDV	Description
07h	bMaxDataInSize	Read/ Persistent	1	40h	Maximum Data In Size (32KB) Maximum data size in a DATA IN UPIU Value expressed in number of 512 Byte units bMaxDataInSize shall not exceed the bMaxInBufferSize parameter. bMaxDataInSize = bMaxInBufferSize when the UFS device is shipped.
08h	bMaxDataOutSize	Read/ Persistent	1	40h	Maximum Data-Out Size (32KB) Maximum data-size in a DATA-OUT UPIU Value expressed in number of 512 Byte units bMaxDataOutSize shall not exceed the bMaxOutBufferSize parameter. bMaxDataOutSize= bMaxOutBufferSize when the UFS device is shipped.
09h	dDynCapNeeded	Read Only	4	0000 0000h	Dynamic Capacity Needed The amount of physical memory needed to be removed from the physical memory resource pool of the particular logical unit, in units of bOptimalWriteBlockSize.
0Ah	bRefClkFreq	Read/ Write Once	1	01h	Reference Clock Frequency Value 0h:19.2MHz 1h: 26MHz 2h: 38.4MHz 3h: 52MHz Others: Reserved
0Bh	bConfigDescrLock	Read/ Write Once	1	00h	Configuration Descriptor Lock 0h: Configuration Descriptor not locked 1h: Configuration Descriptor locked Others: Reserved
0Ch	bMaxNumOfRTT	Read/ Persistent	1	02h	Maximum current number of outstanding RTTs in device that is allowed. bMaxNumOfRTT shall not exceed the bDeviceRTTCap parameter. This parameter can be written by the host only when all LU task queues are empty.
0Dh	wExceptionEventControl	Read/ Volatile	2	0000h	Each bit, if set to '1' by the host, enables the assertion of the relevant exception event bit, allowing the device to raise the EVENT_ALERT bit in the Device Information field in the Response UPIU: 0h: DYNCAP_EVENT_EN 1h: SYSPOOL_EVENT_EN 2h: URGENT_BKOPS_EN Others: Reserved

IDN	NAME	TYPE	Size [Byte]	MDV	Description
0Eh	wExceptionEventStatus	Read Only	2	0000h	Each bit represents an exception event. A bit will be set only if the relevant event has occurred (regardless of the wExceptionEventControl status). 0h: DYNCAP_NEEDED 1h: SYSPOOL_EXHAUSTED 2h: URGENT_BKOPS Others: Reserved
0Fh	dSecondsPassed	Write Only	4	0000 0000h	Bit [31:0]: Seconds passed from TIME BASELINE (see wPeriodicRTCUpdate inDevice Descriptor)
10h	wContextConf	Read/ Volatile	2	0000h	INDEX specifies the LU number. SELECTOR specifies the Context ID within the LU. Valid range: 01h to 0Fh. Bit [15:8]: RFU Bit [7:6]: Reliability mode 00h: MODE0 (normal) 01h: MODE1 (non-Large Unit, reliable mode or Large Unit unit-by-unit mode) 02h: MODE2 (Large Unit, one-unit-tail mode) 03h: Reserved Bit [5:3]: Large Unit multiplier. If Large Unit context is set, this field defines the Large Unit size, else it is ignored Bit [2]: Large Unit context 00b: Context is not following Large Unit rules 01b: Context follows Large Unit rules Bit [1:0]: Activation and direction mode 00b: Context is closed and is no longer active. 01b: Context is configured and activated as a write-only context and according to the rest of the bits in this configuration register. 10b: Context is configured and activated as a read-only context and according to the rest of the bits in this configuration register. 11b: Context is configured and activated as a read/write context and according to the rest of the bits in this configuration register.
11h	Obsoleted	Read Only	4	0000 0000h	Obsoleted
12h~13h	Reserved			-	Reserved for Unified Memory Extension standard

IDN	NAME	TYPE	Size [Byte]	MDV	Description
14h	bDeviceFFUStatus	Read Only	1		Device FFU Status 00h: No information 01h: Successful microcode update 02h: Microcode corruption error 03h: Internal error 04h: Microcode version mismatch 05h~FEh: Reserved 0FFh: General Error
15h	bPSAState	Read/ Persistent	1	00h	00h: 'Off'. PSA feature is off. 01h: 'Pre-soldering'. PSA feature is on, device is in the pre-soldering state. 02h: 'Loading Complete' PSA feature is on. The host will set to this value after the host finished writing data during pre-soldering state. 03h: 'Soldered'. PSA feature is no longer available. Set by the Device to indicate it is in postsoldering state. This attributes unchangeable after it is in 'Soldered' state.
16h	dPSADataSize	Read/ Persistent	1	00h	The amount of data that the host plans to load to all logical units with bPSASensitive set to 1.

9. M-PHY & UniPro Attributes

9.1 M-TX Capability Attributes

Attributes Name	Attribute ID	Default value	Description
TX_HSMODE_Capability	0x01	0x01	[0]: Specifies Support for HS-MODE. 0: False 1: True [7:1]: Reserved The value is set by CoreCfg_TxHSModeCap input.
TX_HSGEAR_Capability	0x02	0x03	[1:0]: Specifies supported HS-GEARS 00: Reserved 01: HS-GEAR1 Only 10: HS-GEAR1 and HS-GEAR2 11: HS-GEAR1, HS-GEAR2, and HS-GEAR3 [7:2]: Reserved The value set by CoreCfg_TxHSGearCap input
TX_PWMG0_Capability	0x03	0x00	PWM-G0 Capability [0]: Specifies Support for PWM-G0 0 – NO 1 – YES [7:1]: Reserved The value set by CoreCfg_TxPWMG0Cap input
TX_PWMGEAR_Capability	0x04	0x05	[2:0]: Specifies supported PWM-GEARS other than PWM 000: Reserved 001: PWM-GEAR1 Only 010: PWM-GEAR1 and PWM-GEAR2 011: PWM-GEAR1 to PWM-GEAR3 100: PWM-GEAR1 to PWM-GEAR4 101: PWM-GEAR1 to PWM-GEAR5 110: PWM-GEAR1 to PWM-GEAR6 111: PWM-GEAR1 to PWM-GEAR7 [7:3]: Reserved The value set by CoreCfg_TxPWMGearCap input
TX_Amplitude_Capability	0x05	0x03	[1:0]: Specifies supported signal amplitude levels 00: Reserved 01: SMALL AMPLITUDE Only 10: LARGE AMPLITUDE Onlly 11: LARGE and SMALL AMPLITUDE [7:2]: Reserved The value set by CoreCfg_TxAmplitudeCap input
TX_ExternalSYNC_Capability	0x06	0x01	[0]: Specifies support for external SYNC pattern. 0: FALSE 1: TRUE [7:1]: Reserved The value set by CoreCfg_TxExtSyncCap. The MPHY DFE doesn't support External SYNC Capability. This should be tied to 1'b0. The DFE sources the SYNC pattern at the beginning of the HS-BURST

Attributes Name	Attribute ID	Default value	Description
TX_HS_Unterminated_ LINE_Drive_Capability	0x07	0x01	[0]: Specifies whether or not M-TX supports driving an unterminated LINE in HS-MODE. 0: NO 1: YES [7:1]: Reserved The value set by CoreCfg_TxHSUnTermDrvCap
TX_LS_Terminated_ LINE_Drive_Capability	0x08	0x01	Specifies whether or not M-TX supports driving an Terminated LINE in LS-MODE. 0: NO 1: YES [7:1]: Reserved The value set by CoreCfg_TxLSTermDrvCap
TX_Min_SLEEP_NoConfig_ Time_Capability	0x09	0x01	[3:0]: Specifies minimum time (in SI) in SLEEP state needed when inline configuration was not performed. Legal values are 0001 to 1111 (1 to 15) [7:4]: Reserved The value set by CoreCfg_TxMinSLEEPNoCfgTime
TX_Min_STALL_NoConfig_ Time_Capability	0x0A	0x01	[7:0]: Specifies minimum time (in SI) in STALL state needed when inline configuration was not performed. Legal values are 01h to FFh (1 to 255) The value set by CoreCfg_TxMinSTALLNoCfgTime
TX_Min_SAVE_Config_ Time_Capability	0x0B	0xFA	[7:0] Specifies minimum reconfiguration time (in 40ns steps). This applies to SLEEP and STALL states Legal values are 01h to FAh (1 to 250) which gives a Maximum time of 10000ns. The value set by CoreCfg_TxMinSAVECfgTime
TX_REF_CLOCK_ SHARED_Capability	0x0C	0x01	[0]: Specifies support for shared reference clock. 0: NO 1: YES [7:1]: Reserved The value set by CoreCfg_TxRefClkShared
TX_PHY_MajorMinor_ Release_Capability	0x0D	0x30	Specifies the major and minor numbers of the M-PHY Version supported by the TX portion of MPHY- [3:0]: Minor Version number. Fixed to 0x0 [7:4]: Major Version Number. Fixed to 0x2 The above values indicate that the MPHY Version of the MPHY Specification.
TX_PHY_Editorial_ Release_Capability	0x0E	0x01	Specifies the sequence number of the M-Phy version supported by the MPHY DFE. [7:0]: This value is fixed to 0x01.

Attributes Name	Attribute ID	Default value	Description
TX_Hibern8Time_ Capability	0x0F	0x01	[7:0]: Specifies the minimum time (in 100 us steps) in HIBERN8 State. Legal values are 01h to 80h (1 to 128) which gives a range of 100us to 12.8ms. The value set by CoreCfg_TxHibern8Time
TX_Advanced_ Granularity_Capability	0x10	0x01	Support and degree of fine granularity steps for a reduced time in HIBERN8 state. If a finer granularity is specified, all coarser granularities shall be supported. [0]: supports fine granularity steps 0: NO (100 µs step) 1: YES [2:1]: step size 00: 4 µs 01: 8 µs 10:16 µs 11: 32 µs Others : Reserved
TX_Advanced_ Hibern8time_Capability	0x11	0x01	Specifies minimum time in HIBERN8 state when advanced granularity is supported in steps defined by TX_Advanced_Granularity_Capability. Existence depends on: TX_Advanced_Granularity_Capability [7:0]: 1 to 128
TX_HS_Equalizer_ Setting_Capability	0x12	0x03	Support for transmit path de-emphasis for HS-MODE Existence depends on: TX_HSMODE_Capability [0] 0: De-emphasis of 3.5dB not supported, 1: De-emphasis of 3.5dB supported, [1] 0: De-emphasis of 6dB not supported, 1: De-emphasis of 6dB supported

9.2 M-RX Capability Attributes

Attributes Name	Attribute ID	Default value	Description
RX_HSMODE_Capability	0x81	0x01	[0]: Specifies Support for HS-MODE 0: False 1: True [7:1]: Reserved The value is set by CoreCfg_RxHSModeCap
RX_HSGEAR_Capability	0x82	0x03	[1:0]: Specifies supported HS-GEARS 00: Reserved 01: HS-GEAR1 Only 10: HS-GEAR1 and HS-GEAR2 11: HS-GEAR1, HS-GEAR2, and HS-GEAR3 [7:2]: Reserved The value set by CoreCfg_RxHSGearCap
RX_PWMG0_Capability	0x83	0x00	[0]: Specifies Support for PWM-G0 0: NO 1: YES [7:1]: Reserved The value set by CoreCfg_RxPWMG0Cap
RX_PWMGEAR_Capability	0x84	0x05	[2:0]: Specifies supported PWM-GEARS other than PWM-G0 000: Reserved 001: PWM-GEAR1 Only 010: PWM-GEAR1 to PWM-GEAR2 011: PWM-GEAR1 to PWM-GEAR3 100: PWM-GEAR1 to PWM-GEAR4 101: PWM-GEAR1 to PWM-GEAR5 110: PWM-GEAR1 to PWM-GEAR6 111: PWM-GEAR1 to PWM-GEAR7 [7:3]: Reserved The value set by CoreCfg_RxPWMGearCap
RX_HS_Unterminated_ Capability	0x85	0x01	[0]: Specifies support for disconnection of resistive termination in HS-MODE. 0: NO 1: YES [7:1]: Reserved The value set by CoreCfg_RxHSUnTermCap
RX_LS_Terminated_ Capability	0x86	0x01	[0]: Specifies support for enabling resistive termination in LS-Mode. 0: NO 1: YES [7:1]: Reserved The value set by CoreCfg_RxLSTermCap

Attributes Name	Attribute ID	Default value	Description
RX_Min_SLEEP_NoConfig_ Time_Capability	0x87	0x01	[3:0]: Specifies minimum time (in SI) in SLEEP state needed when inline configuration was not performed. Legal values are 0x01 to 0x0F (1 to 15) [7:4]: Reserved The value set by CoreCfg_RxMinSLEEPNoCfgTime
RX_Min_STALL_NoConfig_ Time_Capability	0x88	0x08	[7:0]: Specifies minimum time (in SI) in STALL state needed when inline configuration was not performed. Legal values are 0x01 to 0xFF (1 to 255) The value set by CoreCfg_RxMinSTALLNoCfgTime
RX_Min_SAVE_Config_ Time_Capability	0x89	0xFA	Specifies minimum reconfiguration time (in 40 ns steps). This applies only to SLEEP and STALL states. [7:0]: Specifies minimum reconfiguration time (in 40ns steps). This applies to SLEEP and STALL states Legal values are 01h to FAh (1 to 250) which gives a maximum time of 10000ns. The value set by CoreCfg_RxMinSAVECfgTime M-RX needs save config time longer than its RX_Min_SAVE_Config_Time_Capability (realistic : 0x400)
RX_REF_CLOCK_ SHARED_Capability	0x8A	0x01	[0]: Specifies support for shared reference clock 0: NO 1: YES [7:1]: Reserved The value set by CoreCfg_RxRefClkShared
RX_HS_G1_SYNC_ LENGTH_Capability	0x8B	0x03	[5:0]: Sync Length (0 to 15) [7:6]: SYNC Range 00: FINE 01: COARSE The value set by CoreCfg_RxHSG1SyncLength
RX_HS_G1_PREPARE_ LENGTH_Capability	0x8C	0x08	[3:0]: HS GEAR1 PREPARE Length Multiplier for MPHY-DFE (0 to 15) [7:4]: Reserved The value set by CoreCfg_RxHSG1PrepareLength
RX_LS_PREPARE_LENGTH_ Capability	0x8D	0x01	[3:0]: PWM-Burst or SYS-Burst PREPARE Length Multiplier for MPHY-DFE (0 to 15) [7:4]: Reserved The value set by CoreCfg_RxLSPrepareLength
RX_PWM_Burst_Closure_ Length_Capability	0x8E	0x0A	Specifies minimum burst closure time (in SI) necessary to guarantee complete data processing inside M-RX [7:0]: BURST CLOSURE sequence duration in SI. The value set by CoreCfg_RxPWMBurstClosure M-RX needs burst closure time longer than its RX_PWM_Burst_Closure_Length_Capability (realistic : 0x10)

Attributes Name	Attribute ID	Default value	Description
RX_Min_ActivateTime_ Capability	0x8F	0x07	[3:0]: Specifies minimum activate time needed in 100us steps (1 to 15) [7:4]: Reserved The value set by CoreCfg_RxPWMBurstClosure Even though RX_Min_ActivateTime_Capability is 0x1, it sends MinActivate in PACP_CAP_EXT1_ind with 0x4
RX_PHY_MajorMinor_ Release_Capability	0x90	0x30	Specifies the major and minor numbers of the M-PHY Version supported by the RX portion of MPHY-DFE. [3:0]: Minor Version number. Fixed to 0x0 [7:4]: Major Version Number. Fixed to 0x2 The above values indicate that the MPHY-DFE supports 2.00 Version of the MPHY Specification.
RX_PHY_Editorial_ Release_Capability	0x91	0x01	Specifies the sequence number of the M-PHY version supported by the MPHY DFE. [7:0]: This value is fixed to 0x01.
RX_Hibern8Time_ Capability	0x92	0x10	[7:0]: Specifies the minimum time (in 100us steps) in HIBERN8 State. Legal values are 0x01 to 0x80 (1 to 128) which gives a range of 100us to 12.8ms. The value set by CoreCfg_RxHibern8Time Even though RX_Hibern8Time_Capability is 0x1, it sends THibern8 in PACP_CAP_EXT1_ind with 0xA
RX_PWM_G6_G7_SYNC_ LENGTH_Capability	0x93	0x00	Synchronization pattern length, in SI, for PWM-G6 and PWM-G7 in LS-MODE . Existence depends on: RX_PWMGEAR_Capability [5:0]: Sync Length (0 to 15) [7:6]: SYNC Range 00: FINE 01: COARSE The value set by CoreCfg_RxPWMG6G7SyncLength
RX_HS_G2_SYNC_ LENGTH_Capability	0x94	0x03	High Speed GEAR 3 Synchronization pattern length in SI. Existence depends on: RX_HSGEAR_Capability [5:0]: Sync Length (0 to 15) [7:6]: SYNC Range 00: FINE 01: COARSE The value set by CoreCfg_RxHSG2SyncLength
RX_HS_G3_SYNC_ LENGTH_Capability	0x95	0x03	High Speed GEAR 3Synchronization pattern length in SI. Existence depends on: RX_HSGEAR_Capability [5:0]: Sync Length (0 to 15) [7:6]: SYNC Range 00: FINE 01: COARSE The value set by CoreCfg_RxHSG3SyncLength

Attributes Name	Attribute ID	Default value	Description
RX_HS_G2_PREPARE_ LENGTH_Capability	0x96	0x05	HS-G2 PREPARE length multiplier for M-RX. Existence depends on: RX_HSGEAR_Capability [3:0]: 0 to 15 [7:4]: Reserved
RX_HS_G3_PREPARE_ LENGTH_Capability	0x97	0x03	HS-G3 PREPARE length multiplier for M-RX. Existence depends on: RX_HSGEAR_Capability [3:0]: 0 to 15 [7:4]: Reserved The value set by CoreCfg_RxHSG3PrepareLength
RX_advanced_ granularity_capability	0x98	0x07	Support and degree of fine granularity steps for THIBERN8 and TACTIVATE. [0]: supports fine granularity steps 0: No (100 µs step) 1: Yes [2:1]: step size 00: 4 µs 01: 8 µs 10: 16 µs 11: 32 µs Even though RX_Advanced_Granularity_Capability is 0x1, it sends RxAdvGranularity in PACP_CAP_EXT1_ind with 0x5
RX_advanced_ hibern8time_capability	0x99	0x20	Specifies minimum time in HIBERN8 state when advanced granularity is supported in steps defined by RX_advanced_Granularity_Capability. Existence depends on: RX_Advanced_Granularity_Capability Range : 1 to 128 Even though RX_Advanced_Hibern8Time_Capability is 0x4, it sends TAdvHibern8 in PACP_CAP_EXT1_ind with 0x20
RX_advanced_min_ activatetime_capability	0x9A	0x0E	Specifies minimum activate time when advanced granularity is supported in steps defined by RX_Advanced_Granularity_Capability. Existence depends on: RX_Advanced_Granularity_Capability Range : 1 to 14 Even though RX_Advanced_Min_ActivateTime_Capability is 0x7, it sends TMinActivate in PACP_CAP_EXT1_ind with 0xF

9.3 M-TX Configuration Attributes

Attributes Name	Attribute ID	Default value	Description
TX_MODE	0x21	0x01	Operating Mode [1:0]: Controls the operating mode of the Transmit MPHYDFE. 01: LS_MODE 10: HS_MODE [7:2]: Reserved (default: LS_MODE)
TX_HSRATE_Series	0x22	0x01	[1:0]: Controls the HS Rate Series (Rate A/B) of the Transmit MPHY-DFE. 01: RATE-A 10: RATE-B [7:2]: Reserved (default: RATE-A)
TX_HSGEAR	0x23	0x01	[1:0]Controls the HS-Gear of the Transmit MPHY-DFE. 01: HS-GEAR1 10: HS-GEAR2 11: HS-GEAR3 [7:2]: Reserved (default: HS-GEAR1)
TX_PWMGEAR	0x24	0x01	[2:0]: Controls the PWM-Gear of the Transmit MPHY-DFE. 000: PWM-GEAR0 001: PWM-GEAR1 010: PWM-GEAR2 011: PWM-GEAR3 100: PWM-GEAR4 101: PWM-GEAR5 110: PWM-GEAR6 111: PWM-GEAR7 [7:3]: Reserved (default: PWM-GEAR1)
TX_Amplitude	0x25	0x02	[0]: Controls the Drive Strength of the AFE Outputs on Transmit. 01: SMALL_AMPLITUDE 10: LARGE_AMPLITUDE [7:1]: Reserved (default: LARGE_AMPLITUDE)
TX_HS_SlewRate	0x26	0x00	HS Slew Rate [7:0]: Controls the Slew Rate of the AFE outputs on Transmit. Values of 0x00 to 0xFF can be programmed. (default: 00h)
TX_SYNC_Source	0x27	0x00	[0]: Controls the Source of Synchronization Pattern in the MPHY-DFE 0: INTERNAL_SYNC 1: EXTERNAL_SYNC [7:1]: Reserved The MPHY DFE doesn't support EXTERNAL_SYNC mode. This field should not be written with EXTERNAL_SYNC mode. (default: INTERNAL_SYNC)

Attributes Name	Attribute ID	Default value	Description
TX_HS_SYNC_LENGTH	0x28	0x4F	HS mode Synchronization Pattern Length. [5:0]: Sync Length (0 to 15) [7:6]: SYNC Range 00: FINE 01: COARSE (default: COARSE, 15)
TX_HS_PREPARE_LENGTH	0x29	0x0F	[3:0]: HS PREPARE Length Multiplier for MPHY-DFE (0 to 15) [7:4]: Reserved (default: 15)
TX_LS_PREPARE_LENGTH	0x2A	0x01	[3:0]: PWM-Burst or SYS-Burst PREPARE Length Multiplier for MPHY-DFE (0 to 15) [7:4]: Reserved (default: 10)
TX_HIBERN8_Control	0x2B	0x01	[0]: MPHY-DFE TX HIBERN8 State Control 0: EXIT 1: ENTER [7:1]: Reserved Note: After LINE-RESET condition, the value is reset to EXIT state. (default: ENTER)
TX_LCC_Enable	0x2C	0x01	[0]: Enables the Transmission of LCC at the end of Burst. 0: NO 1: YES [7:1]: Reserved (default: YES)
TX_PWM_BURST_Closure_Extension	0x2D	0x20	[7:0]: BURST CLOSURE sequence duration in SI. (0 to 255) (default: 32)
TX_BYPASS_8B10B_Enable	0x2E	0x00	[0]: Bypass 8b/10b Encoding operation in MPHY-DFE. 0: FALSE 1: TRUE [7:1]: Reserved (default: FALSE)
TX_DRIVER_POLARITY	0x2F	0x00	Output Driver Polarity [0]: Output Driver Polarity. 0: NORMAL 1: INVERTED [7:1]: Reserved (default: NORMAL)

Attributes Name	Attribute ID	Default value	Description
TX_HS_Unterminated_ LINE_Drive_Enable	0x30	0x00	[0]: Enables/Disables the unterminated LINE in HS-MODE. 0: NO 1: YES [7:1]: Reserved (default: NO)
TX_LS_Terminated_ LINE_Drive_Enable	0x31	0x00	[0]: Enables/Disables the terminated LINE in LS-MODE. 0: NO 1: YES [7:1]: Reserved (default: NO)
TX_LCC_Sequencer	0x32	0x0	LCC Sequencer bits [0]: LCC READ-CAPABILITY 0: Not Requested 1: Requested [1]: LCC READ-MFG-INFO 0: Not Requested 1: Requested [2]: LCC READ-VEND-INFO 0: Not Requested 1: Requested [6:3] Reserved [7]: LCC WRITE-ATTRIBUTE 0: Not Requested 1: Requested (default: No READ or WRITE operation Requested)
TX_Min_ActivateTime	0x33	0xF	[3:0]: Specifies minimum activate time needed in 100us steps (1 to 15) [7:4]: Reserved (default: 15)
TX_PWM_G6_G7_SYNC_ LENGTH	0x34	0x4F	PWM G6/G7 mode Synchronization Pattern Length. [5:0]: Sync Length (0 to 15) [7:6]: SYNC Range 00: FINE 01: COARSE (default: COARSE, 15)
TX_Advanced_ Granularity_Step	0x35	0x0	Support and degree of fine granularity steps for TACTIVATE Reset Value: 0 [0]: Supports advanced granularity 0: NO 1: YES [2:1] step size 00: 4 µs 01: 8 µs 10: 16 µs 11: 32 µs Others: Reserved

Attributes Name	Attribute ID	Default value	Description
TX_Advanced_Granularity	0x36	0xF	Specifies minimum activate time when advanced granularity is supported in steps defined by TX_Advanced_Granularity_Step. [3:0]: 1 to 15 Others: Reserved
TX_HS_Equalizer_Setting	0x37	0x0	HS Transmit path de-emphasis value selection. Existence depends on: TX_HSMODE_Capability AND TX_HS_Equalizer_Setting_Capability. Value depends on: TX_HS_Equalizer_Setting_Capability Required Values: Support for de-emphasis of 3.5 dB or 6 dB Reset Value: 0 for local RESET. LINE-RESET shall not reset the value of this attribute.
TX_FSM_State	0x41	0x1	To read out the current state of M-TX 0: DISABLED 1: HIBERN8 2: SLEEP 3: STALL 4: LS-BURST 5: HS-BURST 6: LINE-CFG 7: LINE-RESET

9.4 M-RX Configuration Attributes

Attributes Name	Attribute ID	Default value	Description
RX_MODE	0xA1	0x01	Operating Mode [1:0]: Controls the operating mode of the Receive MPHYDFE. 01: LS_MODE 10: HS_MODE [7:2]: Reserved (default: LS_MODE)
RX_HSRATE_Series	0xA2	0x01	[1:0]: Controls the HS Rate Series (Rate A/B) of the Receive MPHY-DFE. 01: RATE-A 10: RATE-B [7:2]: Reserved (default: RATE-A)
RX_HSGEAR	0xA3	0x01	[1:0]: Controls the HS-Gear of the Receive MPHY-DFE. 01: HS-GEAR1 10: HS-GEAR2 11: HS-GEAR3 [7:2]: Reserved (default: HS-GEAR1)
RX_PWMGEAR	0xA4	0x01	[2:0]: Controls the PWM-Gear of the Receive MPHY-DFE. 000: PWM-GEAR0 001: PWM-GEAR1 010: PWM-GEAR2 011: PWM-GEAR3 100: PWM-GEAR4 101: PWM-GEAR5 110: PWM-GEAR6 111: PWM-GEAR7 [7:3]: Reserved (default: PWM-GEAR1)
RX_LS_Terminated_Enable	0xA5	0x00	[0]: Enables/Disables the resistive termination of Receive in LS-MODE. 0: OFF 1: ON [7:1]: Reserved (default: OFF)
RX_HS_Unerminated_ Enable	0xA6	0x00	[0]: Enables/Disables the resistive termination of Receive in HS-MODE. 0: OFF 1: ON [7:1]: Reserved (default: OFF)

Attributes Name	Attribute ID	Default value	Description
RX_Enter_HIBERN8	0xA7	0x01	HIBERN8 Control [0]: MPHY-DFE RX Entry to HIBERN8 State 0: NO 1: YES [7:1]: Reserved Note: After LINE-RESET condition, the value is reset to NO state. (default: YES)
RX_BYPASS_8B10B_Enable	0xA8	0x00	[0]: Bypass 8b/10b decoding operation in MPHY-DFE. 0: FALSE 1: TRUE [7:1]: Reserved (default: FALSE)

9.5 M-TX & M-RX Status Attributes

Attributes Name	Attribute ID	Default value	Description
TX_FSM_State	0x41	0x00	[3:0]: Current State of TX FSM in MPHY-DFE 000: DISABLED 001: HIBERN8 010: SLEEP 011: STALL 100: LS-BUSRT 101: HS-BURST 110: LINE-CFG 111: LINE-RESET
RX_FSM_State	0xC1	0x00	[3:0]: Current State of RX FSM in MPHY-DFE 000: DISABLED 001: HIBERN8 010: SLEEP 011: STALL 100: LS-BUSRT 101: HS-BURST 110: LINE-CFG 111: LINE-RESET

9.6 UniPro L1.5 Attributes

Attributes Name	Attribute ID	Default value	Description
PA_PHY_Type	0x1500	0x01	0h: D-PHY 1h: M-PHY
PA_AvailTxDataLanes	0x1520	0x02	1: 1 lane 2: 2 lanes 3: 3 lanes 4: 4 lanes
PA_AvailRxDataLanes	0x1540	0x02	1: 1 lane 2: 2 lanes 3: 3 lanes 4: 4 lanes
PA_MinRxTrailingClocks	0x1543	0x40	Minimum number of PHY byte clock cycles without data to receive before a mode change
PA_TxHsG1SyncLength	0x1552	0x4F	Updated at linkstartup with RxHsG1SyncLength of PACP_CAP_EXT1_ind from host
PA_TxHsG1PrepareLength	0x1553	0xF	Updated at linkstartup with RxHsG1PrepareLength of PACP_CAP_EXT1_ind from host
PA_TxHsG2SyncLength	0x1554	0x4F	Updated at linkstartup with RxHsG2SyncLength of PACP_CAP_EXT1_ind from host
PA_TxHsG2PrepareLength	0x1555	0xF	Updated at linkstartup with RxHsG2PrepareLength of PACP_CAP_EXT1_ind from host
PA_TxHsG3SyncLength	0x1556	0x4F	Updated at linkstartup with RxHsG3SyncLength of PACP_CAP_EXT1_ind from host
PA_TxHsG3PrepareLength	0x1557	0xF	Updated at linkstartup with RxHsG3PrepareLength of PACP_CAP_EXT1_ind from host
PA_TxMk2Extension	0x155A	0x0	
PA_PeerScrambling	0x155B	0x0	
PA_TxSkip	0x155C	0x0	
PA_TxSkipPeriod	0x155D	0xFA	
PA_LocalTxLccEnable	0x155E	0x1	
PA_PeerTxLccEnable	0x155F	0x1	Updated at linkstartup with Status[3] of PACP_CAP_EXT1_ind from host
PA_ActiveTxDataLanes	0x1560	0x1	Active TX Data Lanes(Fast_state) 1: one lane active 2: two lanes active 3: three lanes active 4: four lanes active

Attributes Name	Attribute ID	Default value	Description
PA_ConnectedTxDataLanes	0x1561	0x0	Number of TX Data Lanes connected 0: not connected 1: 1 lane 2: 2 lanes 3: 3 lanes 4: 4 lanes. Updated at linkstartup
PA_TxTrailingClocks	0x1564	0xFF	Number of PHY byte clock cycles forced without data before a mode change from FAST_STATE or SLOW_STATE to SLEEP_STATE. Updated at linkstartup with MinRxTrailingClocks of PACP_CAP_EXT1_ind from host
PA_TxPWRStatus	0x1567	0x3	TX power state status 000: Off state 001: Fast state 010: Slow state 011: Hibernate state 100: Sleep state
PA_TxGear	0x1568	0x1	TX Gear in PWM or HS Mode 001: PWM_G1 or HS_G1 010: PWM_G2 or HS_G2 011: PWM_G3 or HS_G3 100: PWM_G4 101: PWM_G5 110: PWM_G6 111: PWM_G7
PA_TxTermination	0x1569	0x0	FALSE: 0 TRUE: 1
PA_HSSeries	0x156A	0x1	TX and RX Frequency Series in High Speed Mode A:1 B:2
PA_ActiveTxDataLanes	0x1571	0x55	TX/RX power mode TX[b3:b0] RX[b7:b4] 0000: Off mode 0001: Fast mode 0010: Slow mode 0100: Fast auto mode 0101:Slow auto mode 1111: UNCHANGED.

Attributes Name	Attribute ID	Default value	Description
PA_ActiveRxDataLanes	0x1580	0x1	Active RX Data Lanes(Fast_state) 1: one lane active 2: two lanes active 3: three lanes active 4: four lanes active
PA_ConnectedRxDataLanes	0x1581	0x0	Number of RX Data Lanes connected 0: not connected 1: 1 lane 2: 2 lanes 3: 3 lanes 4: 4 lanes Updated at linkstartup
PA_RxPWRStatus	0x1582	0x4	RX power state status 000: Off state 001: Fast state 010: Slow state 011: Hibernate state 100: Sleep state
PA_RxGear	0x1583	0x1	RX Gear in PWM or HS Mode 001: PWM_G1 or HS_G1 010: PWM_G2 or HS_G2 011: PWM_G3 or HS_G3 100: PWM_G4 101: PWM_G5 110: PWM_G6 111: PWM_G7
PA_RxTermination	0x1584	0x0	FALS: 0 TRUE: 1
PA_Scrambling	0x1585	0x0	
PA_MaxRxPWMGear	0x1586	0x5	Maximum RX Low Speed Gears (PWM) 001: PWM_G1 010: PWM_G2 011: PWM_G3 100: PWM_G4 101: PWM_G5 110: PWM_G6 111: PWM_G7 Updated at linkstartup with MaxPWM of PACP_CAP from host

Attributes Name	Attribute ID	Default value	Description
PA_MaxRxHSGear	0x1587	0x3	Maximum RX High Speed Gears (HS), 0 means no HS available 00: NO_HS 01: HS_G1 10 : HS_G2 11: HS_G3 Updated at linkstartup with MaxHS of PACP_CAP from host
PA_PACPReqTimeout	0x1590	0x3F	Expiration value of the PACP_REQUEST_TIMER when PA is waiting for a cnf Message. The unit is 1 ms. No. of clocks required for timeout = PA_PACPReqTimeout x tx_symbolclk_1us_reg at offset 100h x 1000.
PA_PACPReqEoBTimeout	0x1591	0xF	Expiration value of the PACP_REQUEST_TIMER when PA is waiting for the end of burst. The unit is 1ms. Number of clocks required for timeout = PA_PACPReqEoBTimeout x tx_symbolclk_1us_reg at offset 100h x 1000.
PA_RemoteVerInfo	0x15A0	-	Remote peer's version information. Available after a successful Link Start Up Sequence Updated at linkstartup with VersionInfo of PACP_CAP from host
PA_LogicalLaneMap	0x15A1	0x0	Logical to Physical Lane mapping. Attribute contains a valid value after a successful Link Start Up Sequence Updated at linkstartup
PA_SleepNoConfigTime	0x15A2	0xF	Minimum time to wait between bursts in PWM mode when no new configuration was performed Updated at linkstartup with TSleepNoConfig of PACP_CAP from host
PA_StallNoConfigTime	0x15A3	0xFF	Minimum time to wait between bursts in HS mode when no new configuration was performed Updated at linkstartup with TStallNoConfig of PACP_CAP from host
PA_SaveConfigTime	0x15A4	0xFF	Minimum time to wait between bursts when a new configuration was performed. The unit is 40 ns. tx_symbolclk_ns_reg at offset 100h is used to calculate the required time. Updated at linkstartup with TSaveConfig of PACP_CAP from host.
PA_ RxHSUntermination Capability	0x15A5	0x1	Specifies whether or not the inbound Link supports unterminated line in HS mode 0: FALSE 1: TRUE

Attributes Name	Attribute ID	Default value	Description
PA_ RxLSTerminationCapability	0x15A6	0x1	Specifies whether or not the inbound Link supports terminated line in PWM mode. Updated at linkstartup with THibern8 of PACP_CAP_EXT1_ind from host
PA_Hibern8Time	0x15A7	0x80	Minimum time to wait in HIBERN8 before allowing a M-TX to exit HIBERN8. The unit is 100 us. Number of clocks required for timeout = 100 x PA_Hibern8Time x tx_symbolclk_1us_reg at offset 100h Updated at linkstartup with TMinActivate of PACP_CAP_EXT1_ind from host
PA_TActivate	0x15A8	0xF	Time to wait in SAVE before activating a burst in order to wake up OMC and remote M-RX. The unit is 10 us. No. of clocks required for timeout = 10 x PA_TActivate x tx_symbolclk_1us_reg at offset 100h
PA_LocalVerInfo	0x15A9	0x3	Local version info. Delivered during Link Startup sequence to the peer and stored there to PA_RemoteVerInfo.
PA_Granularity	0x15AA	0x6	Updated at linkstartup with RxAdvGranularity of PACP_CAP_EXT1_ind from host
PA_MK2Extension GuardBand	0x15AB	0x0	
PA_PWRModeUserData [0 to 11]	0x15B0 to 0x15BB	0x00	Data to be sent within PACP_PWR_req and delivered to the remote DME.
PA_PACPFrameCount	0x15C0	0x0	Number of valid PACP frames received.
PA_PACPErrorCount	0x15C1	0x0	Number of erroneous PACP frames received.
PA_PHYTestControl	0x15C2	0x0	

9.7 UniPro L2 Attributes

Attributes Name	Attribute ID	Default value	Description
DL_TxPreemptionCap	0x2000	0x1	
DL_TC0TxMaxSDUSize	0x2001	0x90	
DL_TC0RxInitCreditVal	0x2002	0x7C	
DL_TC1TxMaxSDUSize	0x2003	0x90	
DL_TC1RxInitCreditVal	0x2004	0x0	
DL_TC0TxBufferSize	0x2005	0x80	
DL_TC1TxBufferSize	0x2006	0x0	
DL_TC0TXFCThreshold	0x2040	0x9	
DL_FC0ProtectionTimeOutVal	0x2041	0x1FFF	
DL_TC0ReplayTimeOutVal	0x2042	0xFFFF	
DL_AFC0ReqTimeOutVal	0x2043	0x7FFF	
DL_AFC0CreditThreshold	0x2044	0x0	
DL_TC0OutAckThreshold	0x2045	0x0	
DL_PeerTC0Present	0x2046	0x0	
DL_PeerTC0RxInitCreditVal	0x2047	0x0	

9.8 UniPro L3 Attributes

Attributes Name	Attribute ID	Default value	Description
N_DeviceID	0x3000	0x1	Local Device ID
N_DevieID_valid	0x3001	0x1	N_Device ID attribute is valid. 0: False 1: True
N_TC0TxMaxSDUSize	0x3020	0x111	Maximum Transmit payload size per packet for TC0

9.9 UniPro L4 Attributes

Attributes Name	Attribute ID	Default value	Description
T_NumCports	0x4000	0x1	No. of available cports
T_NumTestFeatures	0x4001	0x1	No. of available Test Feature instances
T_ConnectionState	0x4020	0x1	State of the connection
T_PeerDeviceID	0x4021	0x0	Device id of the peer cport
T_PeerCportID	0x4022	0x0	CPortID of the peer cport
T_TrafficClass	0x4023	0x0	Traffic Class of current connection
T_TxTokenValue	0x4026	0x20	Value of E2E FC Token transmitted
T_RxTokenValue	0x4027	0x20	Value of E2E FC Token received
T_LocalBufferSpace	0x4028	0x0	Amount of local buffer space
T_PeerBufferSpace	0x4029	0x0	Conservative value of amount of buffer space at the peer cport
T_CreditsToSend	0x402A	0x0	Amount of space in the local buffer that has not been communicated to remote destination port yet
T_CportMode	0x402B	0x1	Cport mode 1: Application 2: Test mode
T_TC0xMaxSDUSize	0x4060	0x110	Maximum Transmit payload size per segment for TC0

9.10 UniPro DME DDB L1 Attrubutes

Attributes Name	Attribute ID	Default value	Description
DME_DDBL1_Revision	0x5000	0x10	The revision of the DDB Specification supported by this Device encoded as major-version * 0x10 + minor-version. The value shall be 0x10. (DDB v1.0).
DME_DDBL1_Level	0x5001	0x1	Eight bit field indicating the DDB support: b0: DDB Level 1 support. Shall be 0b b1: DDB Level 2 get support. Shall be 0b1 if, and only if, the GET-DDB-LEVEL2 Service is supported. If b1 is set to '1', then b0 shall also be set to '1'. b2: DDB Level 2 set support. Shall be 0b1 if, and only if, the SET-DDB-LEVEL2 Service is supported. If b2 is set to '1', both b0 and b1 shall also be set to '1'. b[7:3]: Reserved. Shall be 0b00000.
DME_DDBL1_DeviceClass	0x5002	0x2	The Device Class ID of the DME User as specified by the MIPI Alliance. If the Device does not conform to a specified device class, the value shall be zero
DME_DDBL1_ManufacturerID	0x5003	0x24A	Manufacturer ID of the DME User as specified by the MIPI Alliance.
DME_DDBL1_ProductID	0x5004	0xA00	The Manufacturer's internal product ID of the DME User.
DME_DDBL1_Length	0x5005	0x0	The length of any DDB Level 2 data. For Devices supporting only DDB Level 1, the value shall be zero.

9.11 UniPro TstSrc/TstDst Attributes

Attributes Name	Attribute ID	Default value	Description
T_TstCPortID	0x4080	0x0	The ID of the CPort-under-test
T_TstSrcOn	0x4081	0x0	Message generation state
T_TstSrcPattern	0x4082	0x0	Pattern used for Message generation
T_TstSrcIncrement	0x4083	0x1	The increment value between two consecutive bytes
T_TstSrcMessageSize	0x4084	0x100	The size of each generated Message
T_TstSrcMessageCount	0x4085	0x100	The number of Messages generated (Nonzero: finite Message stream, zero: infinite Message stream).
T_TstSrcInterMessageGap	0x4086	0x0	If non-zero, the gap time between two Messages The actual duration of the timeout period shall be the value set in the attribute ±10%. This value multiplied by SYS1CLK 1us Register (0x0FC) gives the no. of clocks Required
T_TstDstOn	0x40A1	0x0	The state of TstDst
T_TstDstErrorDetectionEnable	0x40A2	0x0	Enable analyzing incoming Messages
T_TstDstPattern	0x40A3	0x0	The expected pattern in the incoming Messages
T_TstDstIncrement	0x40A4	0x1	The expected increment value between two consecutive bytes
T_TstDstMessageCount	0x40A5	0x0	Number of received Messages
T_TstDstMessageOffset	0x40A6	0x0	Offset of error from start of Message
T_TstDstMessageSize	0x40A7	0x100	The expected size of incoming Message
T_TstDstFCCredits	0x40A8	0x100	The amount of credits passed to the flow control Service Primitive
T_TstDstInterFCTokenGap	0x40A9	0x0	The interval in microseconds for which requesting T_CO_FLOWCONTROL.req is skipped. The actual duration of the timeout period shall be the value set in the attribute ±10%. This value multiplied by SYS1CLK 1us Register(0x0FC) gives the no. of clocks required
T_TstDstInitialFCCredits	0x40AA	0x100	The initial number of credits passed by the TstDst to T_CO_FLOWCONTROL.req after enabling the TstDst
T_TstDstErrorCode	0x40AB	0x0	Error code that generated the TstDst disconnection 0: NO_ERROR 1: FRAGMENT_CORRUPT 2: INVALID_MSG_SIZE 3: UNEXPECTED_BYTE_VALUE